A Commodore PET-2001 clone

Built in 2018 using current-production parts.

Glen Kleinschmidt
www.glensstuff.com
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Introduction

This project had its genesis in 2017 when, reading on-line about old computers, I stumbled upon the fact that a variant of the PET-2001's original brain, now more than 40 years old, is still being produced.

The venerable MOS Technology 6502 microprocessor, in its modern guise, is the W65C02S, supplied by fabless semiconductor company Western Design Center, Inc and distributed by Mouser Electronics. WDC specialise in 65xx-brand microprocessor technology and additionally supply the W65C21N and W65C22N, which are, for all practical purposes here, current production, drop-in replacements for the PET's original 6520 "PIA" and 6522 "VIA" chips.

This clone is therefore not another FPGA port or an emulator running on a Raspberry Pi, but a functional replica of the original computer in the traditional hardware sense. Nor is it a part-for-part duplication of the original circuitry, but a complete re-design using contemporary discrete CMOS logic and memory devices, with some additional features thrown in for good measure. At the time or writing every component used in this project is a current-production part.

74HC(T) CMOS family logic almost entirely displaces the original LS TTL logic and great simplifications were made by using modern memory devices. Additionally, although for all practical purposes here the W65C02 is, functionally, entirely equivalent to the original 6502, it is not a direct drop-in replacement. It has slightly different pin functions, different, more stringent timing requirements due to its ability to run several times faster than the original NMOS 6502 and it is a CMOS part with CMOS-level, rather than TTL-level compatible I/O thresholds.

The potential timing incompatibility mostly relates to memory write operations and how briefly (only 10 ns) valid data is guaranteed to remain on the data bus upon the falling edge of the system clock (time T_{HW}). If your memory write strobe decoding doesn't have time to react before the data disappears from the data bus you're going to have trouble with memory write operations! If you peruse my circuit diagrams you'll notice that a pair of 74HCT244 driver chips directly buffer the W65C02S's data I/O pins to the systems data bus. These chips provide CMOS-level to TTL-level threshold conversion and add critical, delayed time extension to T_{HW}. To doubly ensure that the memory write strobe is available well ahead of schedule, it is decoded by a super-fast 74AC family device.

The PET-2001 was originally offered with as little as 4 kilobytes of random access memory, but the BASIC operating system is capable of recognising an expandable maximum of 32 kilobytes. A single modern static RAM chip, part # AS7C256, provides the full 32 kilobytes of system RAM and dispenses with a great deal of address decoding logic. There isn't a need for arrays of 4096-bit memory chips like the old MOS 6550 in this day and age! The scenario is the same for the systems read only memory which stores the operating system. A single AT27C256 chip serves as the system ROM and is in fact large enough to contain both the early and the later revised versions of the BASIC operating system; more about this later.

Back in the day if you wanted sound effects for games (or any other purpose) you would typically connect the CB2 pin at the parallel port of your PET-2001 to the input of an external audio amplifier via an attenuator of some sort. Later models of the PET gained an internal CB2 logic-level-driven speaker, but that I think is a bit rudimentary – for one the volume can't be controlled. My clone design incorporates an LM386 audio amplifier with volume control and a source-select function giving the additional handy utility of letting the user listen in on the read and write signals from or to the external data cassette storage devices.

I also designed a universal “PS/2 keyboard and RS-232 interface”, which is accommodated on a separate, self-contained circuit board and is compatible with any PET-2001, not just my clone design. Via a length of ribbon cable it plugs into the keyboard interface connector and permits the connection of a PS/2 keyboard to the PET and, if desired, communication to the PET via an RS-232 port. The latter function permits you to type to your PET via an ASCII terminal program.

Compete schematic diagrams, bills of material and further technical descriptions follow in this document.

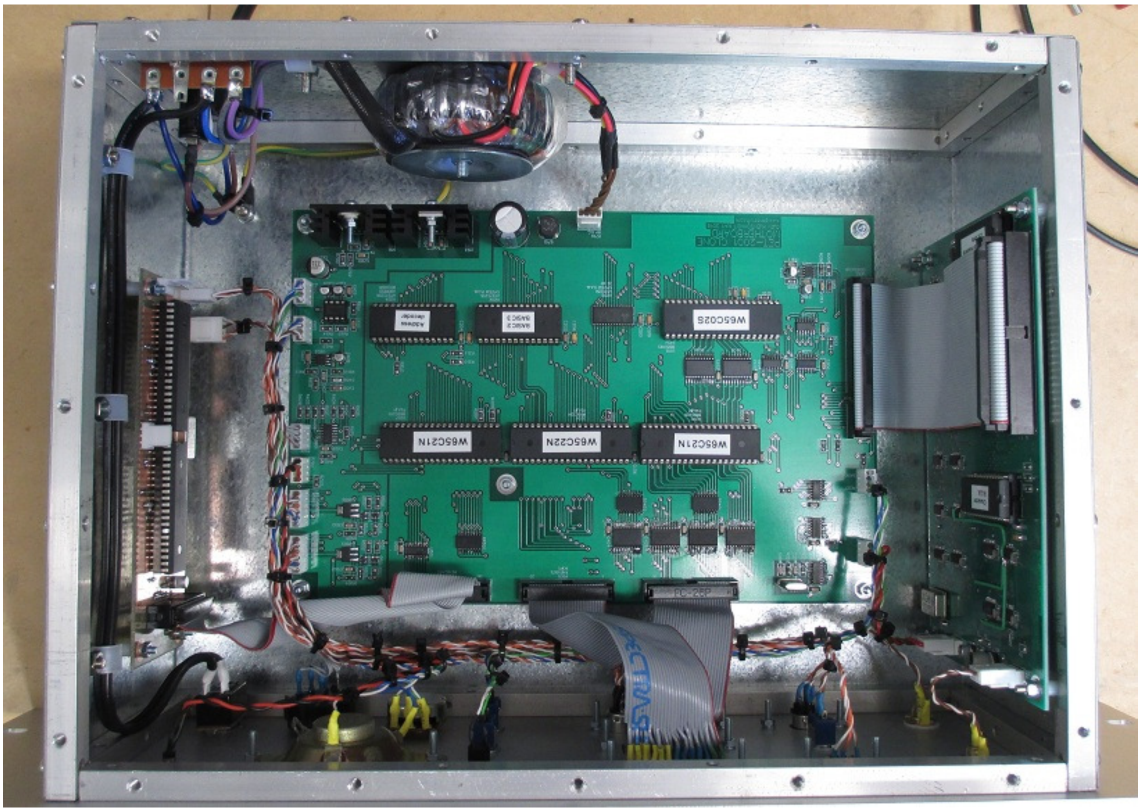
A complete set of Gerber files for the PCBs, ROM image binary files and firmware for the PS/2 keyboard and RS-232 interface unit are available for downloading on my website:

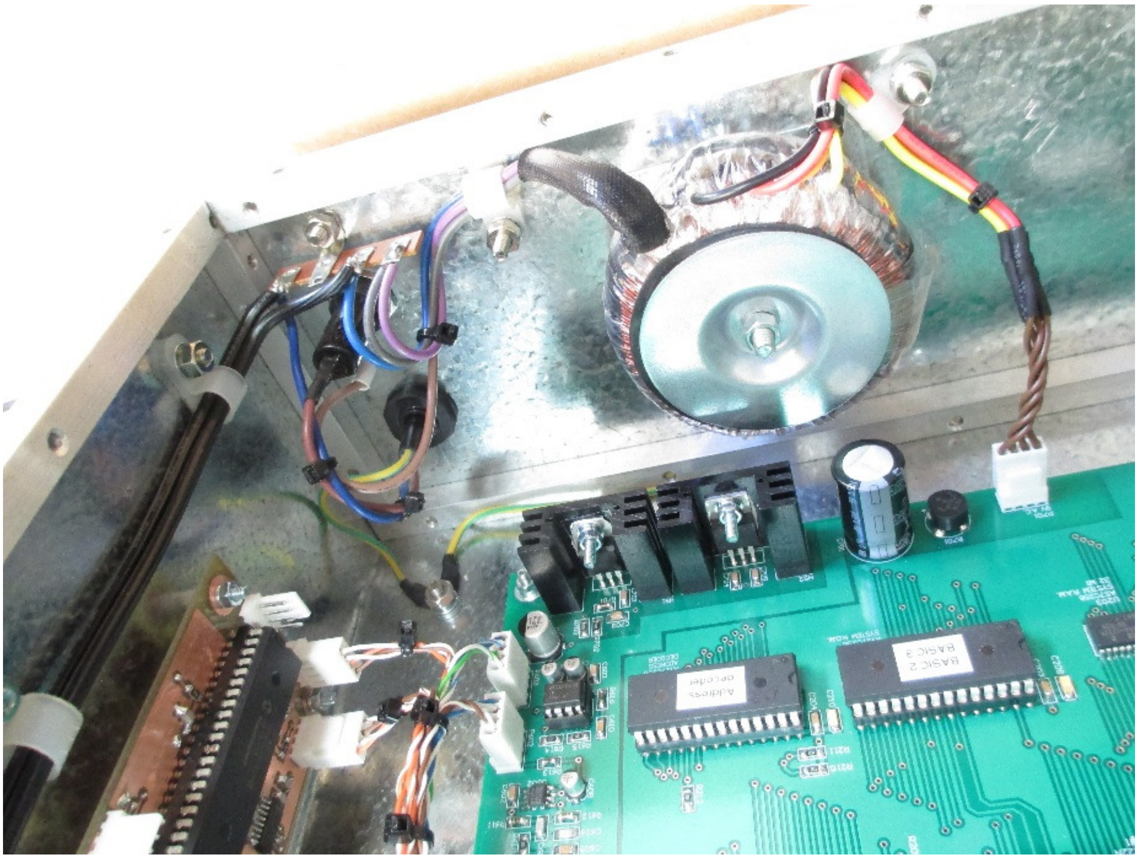
www.glensstuff.com

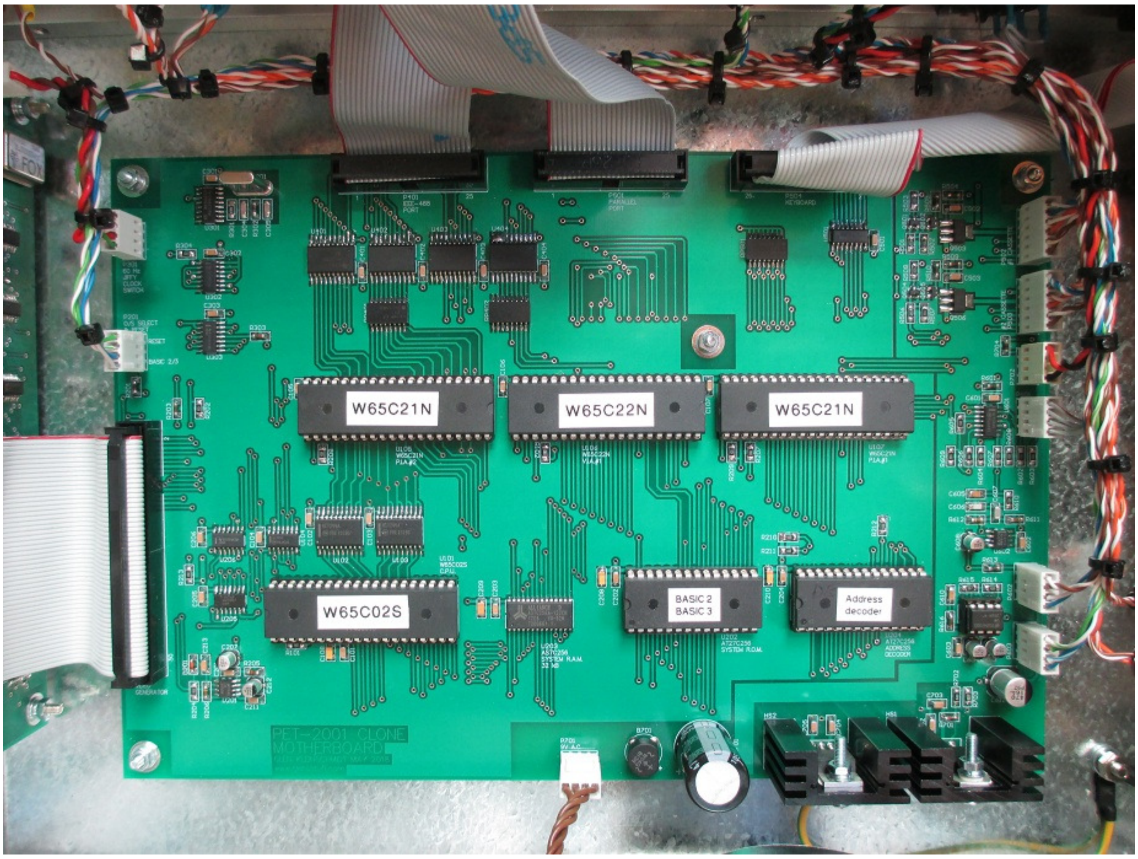
You can view a Youtube video of my competed PET-2001 clone loading and running a version of the computer game *Space Invaders* here:

https://youtu.be/e4uILTKAoj8

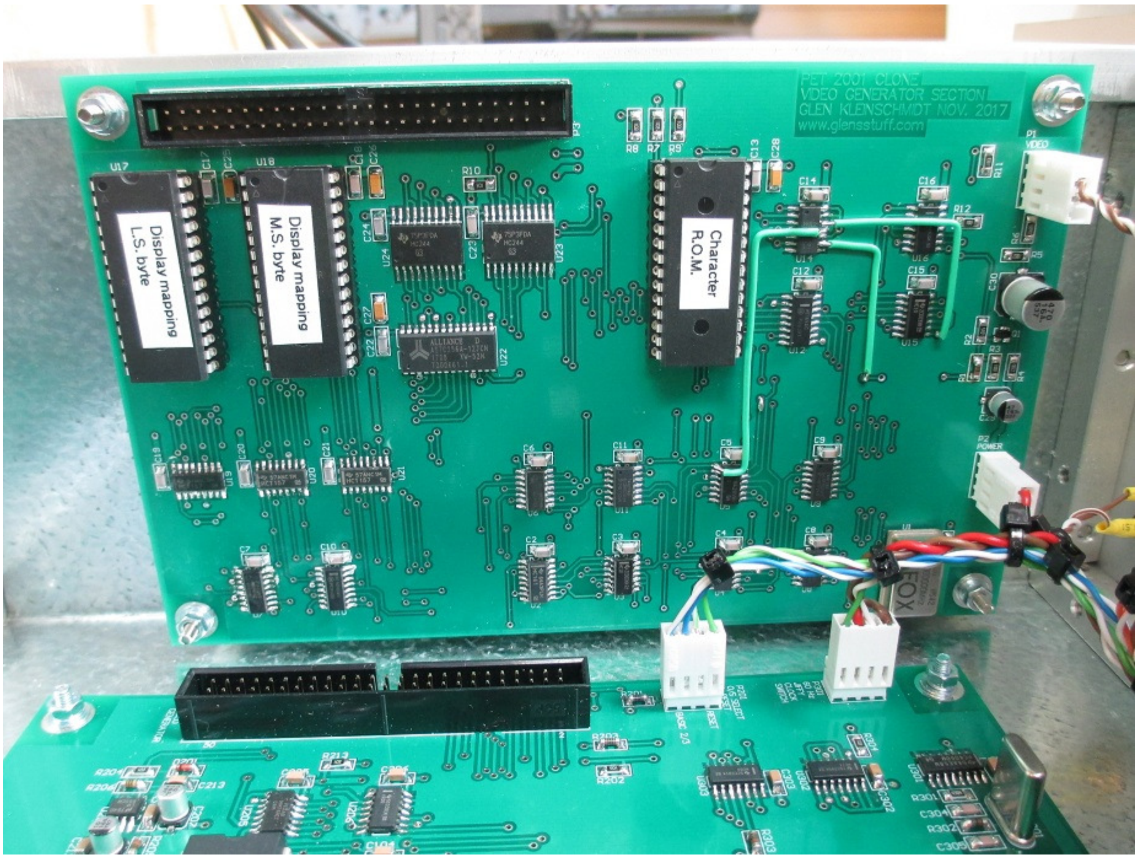

PET-2001 CLONE
PARALLEL PORT
RS-232
VIDEO OUT
RESET
POWER
LEVEL 2
BASIC
LEVEL 3
IEEE-488 PORT
INTERFACE
READ
WRITE
OFF
CB2
JIFFY
CLOCK
CASSETTE #1
CASSETTE #2
AUDIO OUT
COMPAQ


W65C02S
W65C21N
W65C22N
W65C21N

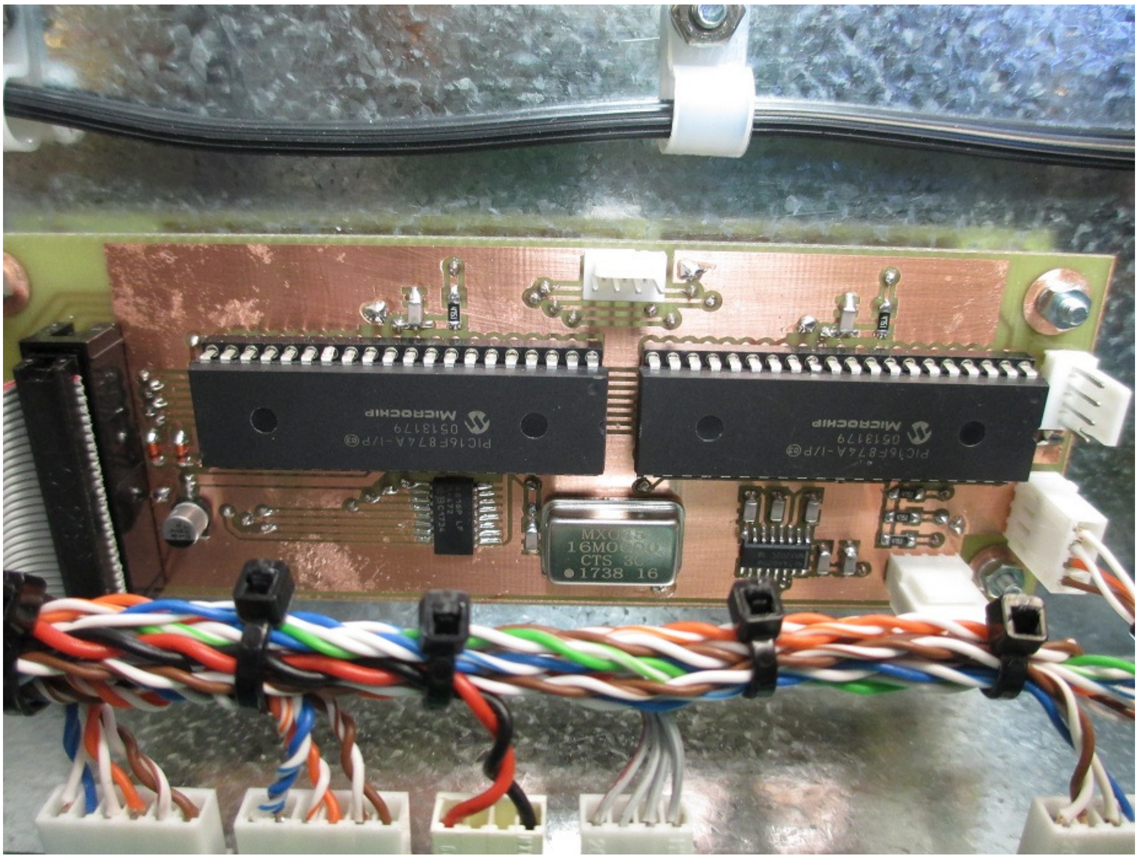




The motherboard



The video generator board


The PS/2 & RS-232 interface board


Muscovy ducks!

Hardware Overview

With the exception of a few power supply components, all of the circuitry in the original PET-2001 was accommodated on one large PCB. In my clone design I have split the video generation circuitry onto a separate PCB. There are thus two PCBs, designated the "motherboard" and the "video generator board".

The motherboard contains:

The power supply circuitry,
CPU,
System RAM & ROM,
VIA and PIA chips,
All peripheral I/O interface circuitry,
Audio amplifier and associated circuitry,
A 60 Hz reference "jiffy" clock/timebase (more about this oddity in a little bit).

Video generator board

The video generator board contains all of the circuity required to generate the PET's 40 column by 25 row, character-based video display. This includes the screen, or video, display RAM, the character ROM and a 16 MHz master oscillator module from which the 1MHz CPU/system clock, as well as all video timing signals, are derived.

Note that in the PET the *video* RAM and ROM space is in addition to and separate from the *system* RAM and ROM space. There are 40 x 25 = 1000 bytes of system-accessible video RAM to define each individual character location. The video ROM simply contains the data defining the PET's unique alpha-numeric and graphical character set and is continuously and exclusively accessed by the circuitry concerned with producing the video display. The video character ROM is not hardware accessible to the CPU.

A significant departure in the video generation circuitry of my clone design, from the PET's original specification, is that, for compatibility with the traditional television displays that we use in this part of the word, I designed for raster refresh rate of 50 Hz (50.08 Hz to be precise, with 312 non-interlaced horizontal lines). The original PET-2001 had its own internal video display monitor that rescanned at a frame rate of 60 Hz, with 260 non-interlaced, horizontal lines. As far as I know, as so far I have not found any evidence to the contrary, Commodore never made a version of the '2001 with an internal video frame rate of 50 Hz.

The first implication of having a video frame rate of 50 Hz rather than 60 Hz is totally inconsequential as far as the actual video display generation is concerned, but as some operations of the CPU are synchronised to the video refresh rate, some functions thus operate at a proportionally slower rate.
A video game program, for example, which synchronises writing to the video RAM during the vertical blanking intervals only, to produce a clean, "snow free" graphical display, will update at the reduced rate. "Snow" was a term given to what was visually produced on the display when the PET is programmed to access the video RAM asynchronously - while the video generation circuitry is busy scribing a visible portion of the display. The PET's snow-free and non snow-free modes of video RAM access were called "slow" and "fast" respectively. The latter was naturally faster because a video RAM read or write didn't have to wait around for the next vertical blanking interval. In reality, however, as far as the 50 Hz vs. 60 Hz difference goes, unless you're sitting next to a 60 Hz PET running the exact same video game at the same time, you'd never be aware of the subtle difference in speed.

The 60 Hz Jiffy clock generator

The second implication of having a video frame rate of 50 Hz rather than 60 Hz, is that the PET's BASIC operating system won't keep accurate time. Now this, obviously, only has an impact upon applications that make use of the PET's internal software real-time clock. The PET measures time in units of 1/60th of a second, dubbed "jiffies". In other words there are 60 jiffies in each second and the video frame rate serves as the timebase. With a timebase of 50 Hz the PET's clock will run about 17% slow.

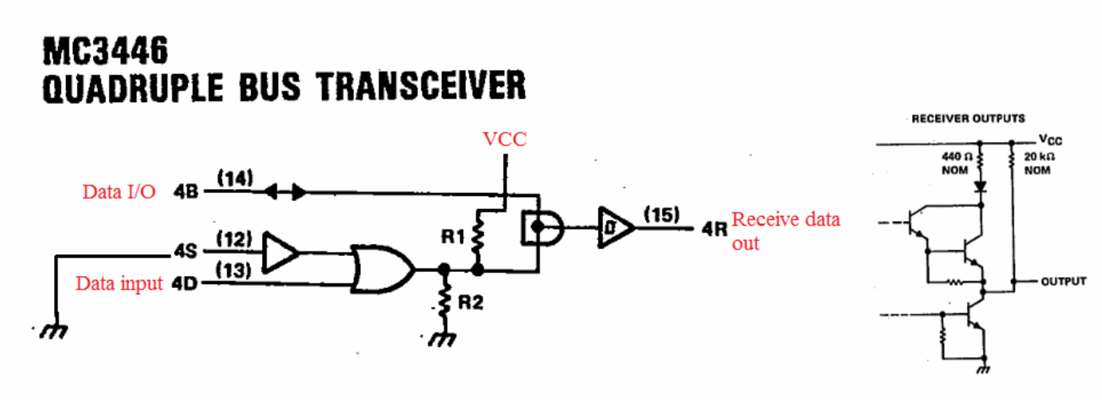
This is the reason why I have included an accurate and alternative 60 Hz timebase clock source on the motherboard. With a flick, one way or the other, of the "Jiffy" switch, CPU synchronisation is derived from either the video vertical refresh rate or from this alternative 60 Hz source. However there is a catch – when switched to the 60 Hz source, the functions of the CPU will no longer be synchronised to the video display and the snow-free modes of video RAM access will cease to be snow-free.

One last issue, which at the time of writing this document I have not had time to fully investigate, is that in the original PET the 60 Hz vertical frame rate, being derived from an 8 MHz master clock by integer division, wasn't therefore precisely 60 Hz. I am led to believe that the PET's OS was programmed with a correction factor to account for this, so that the HH-MM-SS software counter would continue to keep accurate time in the long term.
My alternative jiffy hardware clock, however, is an accurate 60 Hz, so any correction factor applied would accumulate error rather than remove it. I have implemented the accurate alternative jiffy clock this way so as to set myself the challenge of eventually reverse engineering and modifying the operating system ROM to disable any correction factor that may be employed. I am likely not to get around to this for some time though, so if anyone else is up for the challenge or can provide knowledgeable insight, I'd appreciate the feedback.

Referring to sheet 3 of the motherboard schematic set, the 60 Hz jiffy clock is derived from a 3.93216 MHz crystal oscillator divided by 2^{16}. U303 is serves as a 2-input data selector, providing system synchronisation to either the 50 Hz video frame rate or the 60 Hz jiffy clock as commanded by the "Jiffy" frequency selector switch.

IEEE-488 Interface port.

The long-obsolete Motorola IEEE-488 interface chips (MC3446) originally used in the PET were unusual in that a separate receive output pin and transmit input pin were provided for each I/O pin, as opposed to a less cumbersome arrangement utilising a common directional control input.



All I/O, as per the original IEEE-488 standard, was open-collector with resistive (voltage divider) pull-ups to approx. 3.5V. Logic low = true. In these Motorola chips a receive data output pin simply reflected the logic state of its respective I/O pin regardless of whether said I/O pin was asserted true (low) by either an external device or by the respective transmit data input pin being asserted low.

Consequently in the PET there isn't a direction control register of any sort for IEEE-488 communications, but separate output and input register bits for all of the CPU-controlled I/O pins, with the exception of control line SQR, which is an input only and therefore doesn't have an output register address. There are also two control pins which have no register addresses at all as they have no hardware provision for CPU control. These are control lines RET and IFC. The RET line is electrically tied to ground. This asserts the PET as a permanent host. IFC is asserted by the power-on system reset timer only. There are a total of 16 lines in the IEEE-488 standard - 8 data lines and 8 control lines.

To implement the IEEE-488 interface in a manner functionally equivalent to the original PET hardware configuration using current production parts, rather than the obsolete Motorola MC3446, I used a pair of SN75ALS160 IEEE-488 Bus Transceiver chips as the output line drivers and a pair of 74LS245 buffers as the input line receivers. The 74ALS160s chips are wired in uni-directional mode with the active pull-ups disabled. In this mode all I/O pins operate as open-collector outputs with an internal resistive pull-up to ~3.5V.
The 74LS245s are perfect in this application as line receivers as they have the necessary TTL-level input switching thresholds with hysteresis for noise immunity. They also have special high-impedance inputs courtesy of emitter-follower input buffers, so they will not load the internal resistive pull-ups of the SN74ALS160 operating in open-collector mode.

Finally, the receiver outputs of the two 74LS245 chips are connected to PIA#2 and VIA#1 via current-limiting resistors RP401 and RP402. These resistors are necessary because although the PET's BASIC operating system ostensibly configures all PIA and VIA I/O pins connected to the IEEE-488 receiver outputs to be inputs only, there are certain potential scenarios which can cause these pins to be misconfigured as outputs instead, possibly causing contention. While the VIA and PIA chips internally current-limit their I/O pins in the driven high state, the 74LS245 does not. Note that the receiver outputs of the originally-utilised Motorola MC3446 were internally current-limited in the high state by a ~440-ohm resistor in series with the collector of the upper transistor of each output totem-pole.

Audio line-out and power amplifier

The audio circuitry located on the motherboard is quite simple. Referring to page 6 of the motherboard schematic set, U601 is wired as a 1-of 4 data selector under the command of the "Audio source" select switch, which has the following four positions:

Off
Read
Write
CB2

In the off position no data source is selected and the audio is muted. The "Read" position permits the serial data stream received from either data cassette storage unit to be monitored. The "Write" position permits the serial data stream sent to either data cassette storage unit to be monitored. Note that there are separate "read" data lines for each data cassette port, but a common "write" line for both. The two read lines are logically ORed by U601 parts A and B of the audio source data selector.

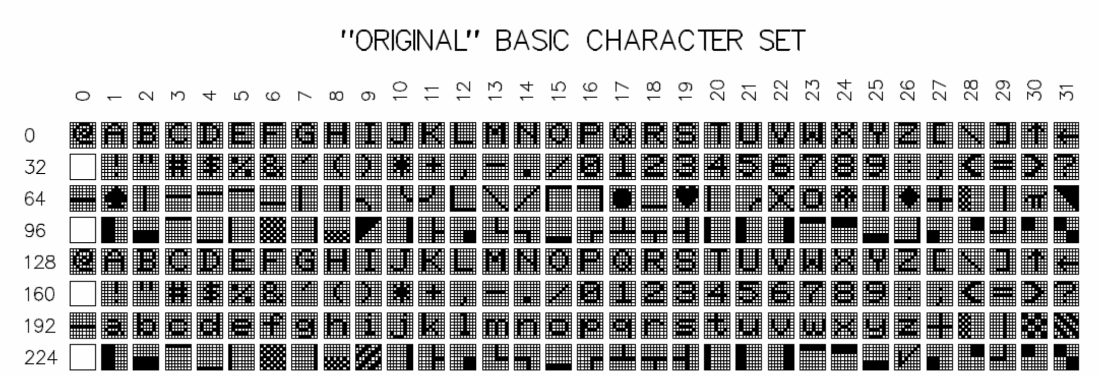
Op-amp U602 serves as a line-level output buffer. The line-level output connects to an RCA jack mounted on the front panel of my clone and serves as an audio output which can handily drive the audio input of a video monitor, if desired. Alternatively the internal amplifier and speaker can be utilised by turning up the volume control. A good old LM386 audio power amplifier, U603, is utilised for speaker-driving duties.

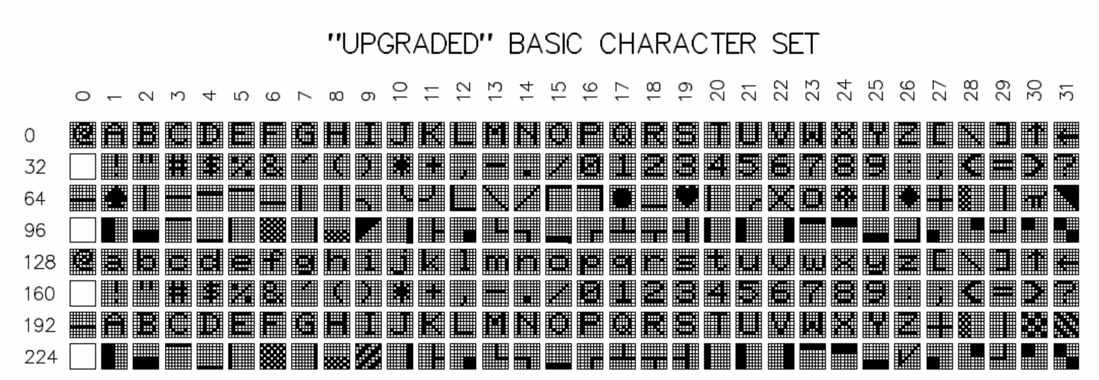
Memory, address decode and BASIC

Referring to page 2 of the motherboard schematic set, U202 is the system ROM. This 32 kilobyte memory contains both versions of the BASIC operating system originally produced for the PET-2001.
Confusingly, the "original" and "upgraded" versions of BASIC are arbitrarily called BASIC 1 and BASIC 2 respectively by some authorities and BASIC 2 and BASIC 3 respectively by others. The former was preferred by Commodore, but others, for example, Donahue & Enger, *PET/CBM Personal Computer Guide*, used the latter:

> The newer ROMs eliminate problems that were encountered with the original ROMs.
> You have Revision 2 ROMs if your PET powers up with the first line printed as:
>
> ***COMMODORE BASIC***
>
> You have Revision 3 ROMs if your PET powers up with the first line printed as:
>
> ###COMMODORE BASIC###

Another thing of note is that at some stage along the line Commodore modified the character ROM:





The character ROM contains 256 individual characters and the PET's video generation hardware splits the ROM into two separate 128 character pages. These pages are called the "Graphics" and "Business" character sets respectively. When switched on the PET boots up using the graphics character set by default. The business page is mostly a duplicate of the graphics page, but substitutes 26 graphics characters with lower case letters of the alphabet.

Both versions of the character ROM are identical, but the updated version swaps around the upper and lower case letters in the business page.

The system ROM, U202, is programmed with the “original” BASIC in the first 16 kilobyte page and “upgraded” BASIC in the other. Page selection is decided by the “BASIC” selector switch which connects to the motherboard via header P201. When the “BASIC” selector switch is open, R202 keeps address pin A14 of U202 low, selecting the lower 16 kilobyte page and thus causing the PET to run “original” BASIC. Closing the “BASIC” selector switch pulls A14 high and selects “upgraded” BASIC.

The “BASIC” selector switch control line also asserts the most significant address bit of the character ROM, U13, of the video generator board. The character ROM is programmed with both character set versions, so that when “original” BASIC is selected the “original” character set will be utilised and when “upgraded” BASIC is selected the “upgraded” character set will be utilised.

Flicking the “BASIC” selector switch while the computer is running will cause the system to crash, but a complete system re-boot can be initiated at any time, without having to cycle the power off and then on again, simply by pressing the “Reset” push button.

Like in the original PET, I used an LM555 Timer I.C. wired as a monostable to generate the power-on system hardware reset. The “Reset” button simply re-triggers the ‘555. The original PET wasn’t provided with a reset button, but many owners back in the day added one themselves, simply to avoid the annoyance of having to reach for the mains power switch each and every time the computer locked up!

All of the computers memory address decoding logic has been simplified to a ROM look-up table stored in U204. There are six separate memory areas accessible to the CPU. These are:

System RAM
Video RAM
System ROM
PIA#1 registers
PIA#2 registers
VIA#1 registers

Power supply

The power supply circuitry is so simple it barely rates a mention. The most important thing of note is that there are two separate regulated supply rails. A +6.3 V rail is produced and used exclusively for powering the motors of the data cassette units and the LM386 audio power amplifier. A +5V logic supply rail is generated to power everything else.

PS/2 keyboard and RS-232 interface.

As the name suggests, this little interface board has two modes of operation. In PS/2 mode (pin RB0 of U2 = high) any PS/2–standard PC keyboard can be used with the PET. It was only a little bit of a challenge to logically and efficiently map all of the PET's functions and unique characters to a modern keyboard layout.

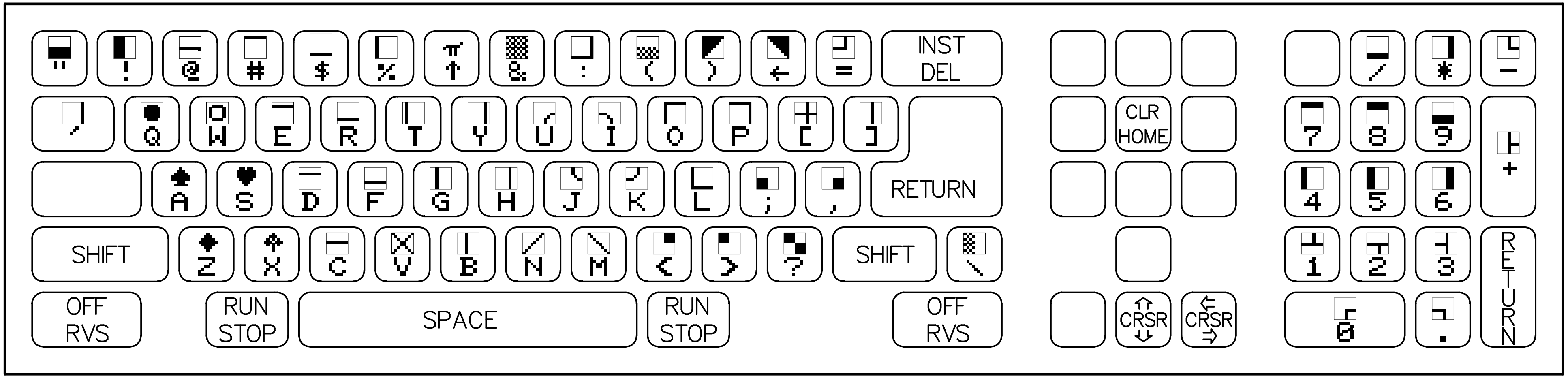
In the page following this written description is a graphical keyboard legend which I produced as a typing aide. I printed this legend out and laminated it, to serve as a handy look-up card when typing. The function keys are easily memorised and after that the card is only really needed when looking for a shifted graphics character. In the PS/2 mode all make and break codes received from the keyboard are echoed out of the RS-232 port at 38400 baud. The mode control switch connects between pins 3 and 4 of header P5.

The second mode of operation (pin RB0 of U2 = low) lets you type to your PET via an RS-232 terminal by receiving standard ASCII character and control codes via the RS-232 port, rather than communicating with a PS/2 keyboard. The ASCII codes are received and immediately echoed back to the terminal at 38400 baud. The only limitation in this mode of operation is that, with the exception of the "pi" character, the PET's shifted graphics characters are otherwise not supported.

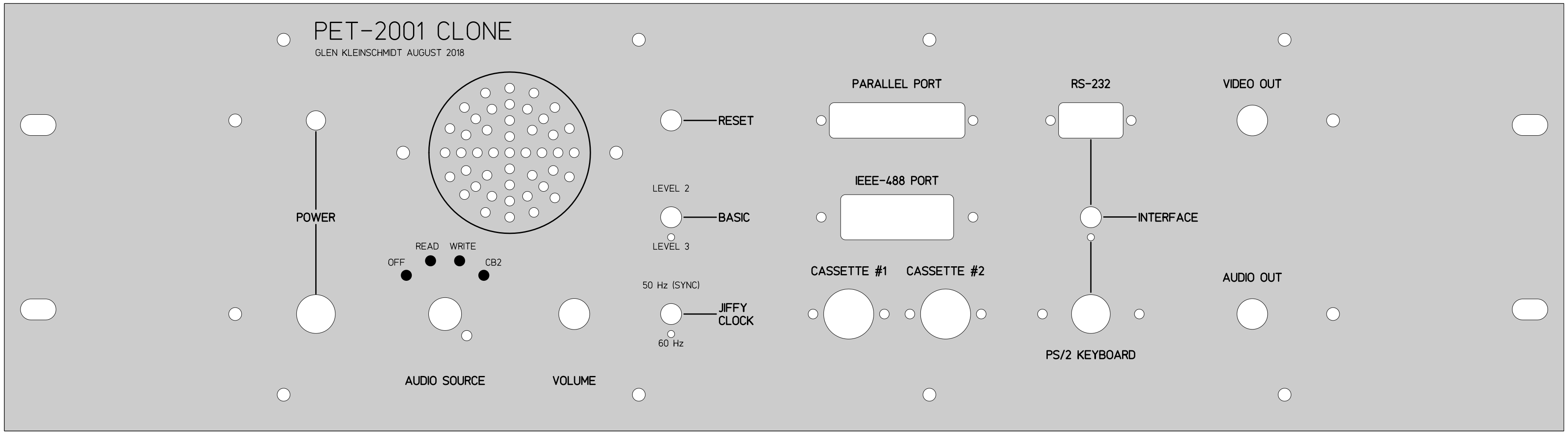
The supported keys and respective ASCII codes are as follows:

Received character	ASCII code (decimal)	PET key / function
H	72	Home cursor
W	87	Cursor up
Z	90	Cursor down
A	65	Cursor left
S	83	Cursor right
C	67	Clear screen
B	66	Stop
N	78	Run
R	82	Reverse on
T	84	Reverse off
I	73	Insert
a	97	A
b	98	B
c	99	C
d	100	D
e	101	E
f	102	F
g	103	G
h	104	H
i	105	I
j	106	J
k	107	K
l	108	L
m	109	M
n	110	N
o	111	O
p	112	P
q	113	Q
r	114	R
s	115	S
t	116	T
u	117	U
v	118	V
w	119	W

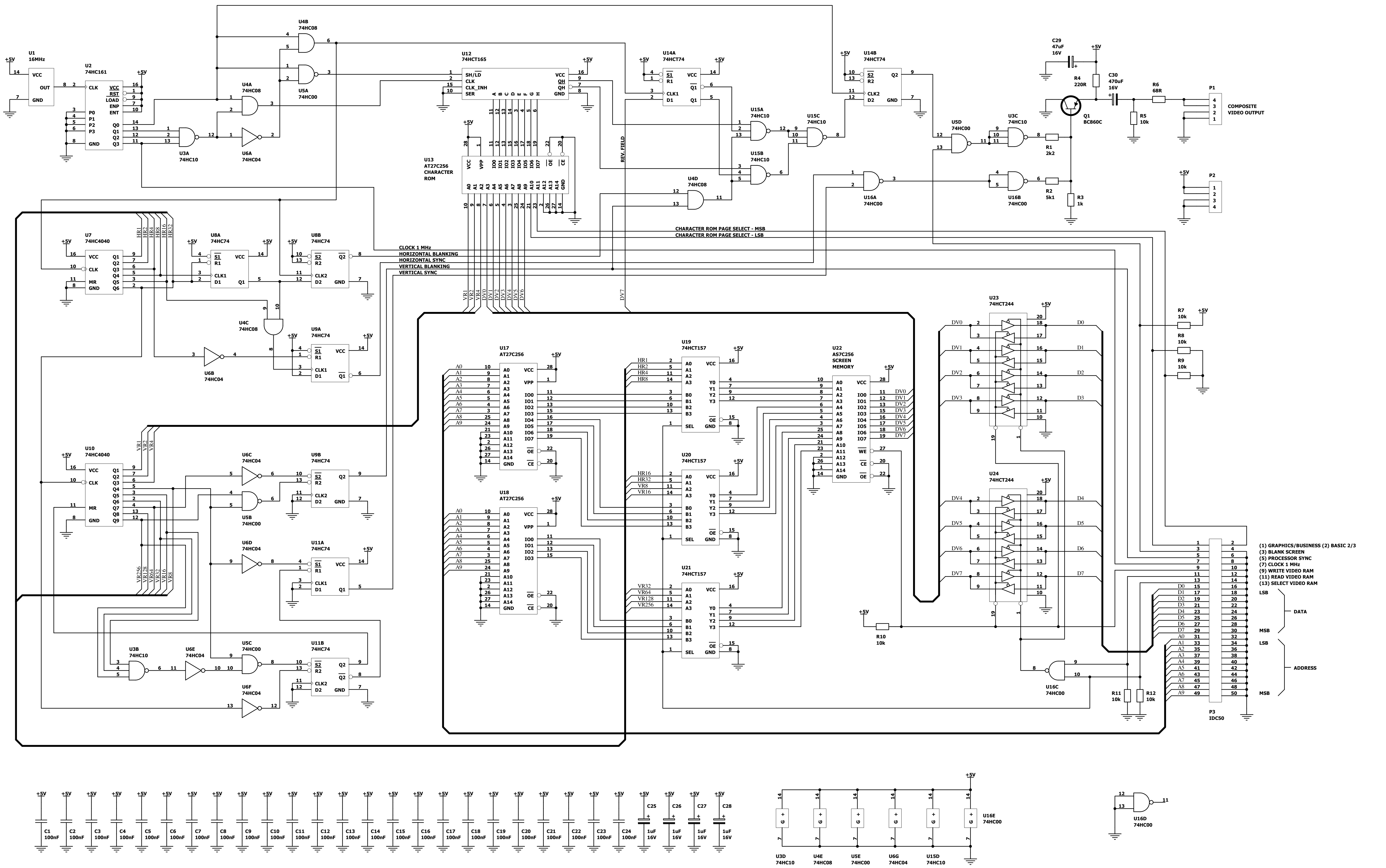
x	120	X
y	121	Y
z	122	Z
0	48	0
1	49	1
2	50	2
3	51	3
4	52	4
5	53	5
6	54	6
7	55	7
8	56	8
9	57	9
+	43	+
-	45	-
=	61	=
[	91	[
]	93	]
<	60	<
>	62	>
!	33	!
@	64	@
#	35	#
$	36	$
%	37	%
^	94	^
&	38	&
*	42	*
(	40	(
)	41	)
_	95	Left arrow symbol
P	80	pi symbol
\	92	\
/	47	/
;	59	;
:	58	:
'	39	'
"	34	"
,	44	,
.	46	.
Enter	13	Return
Backspace	8	Delete

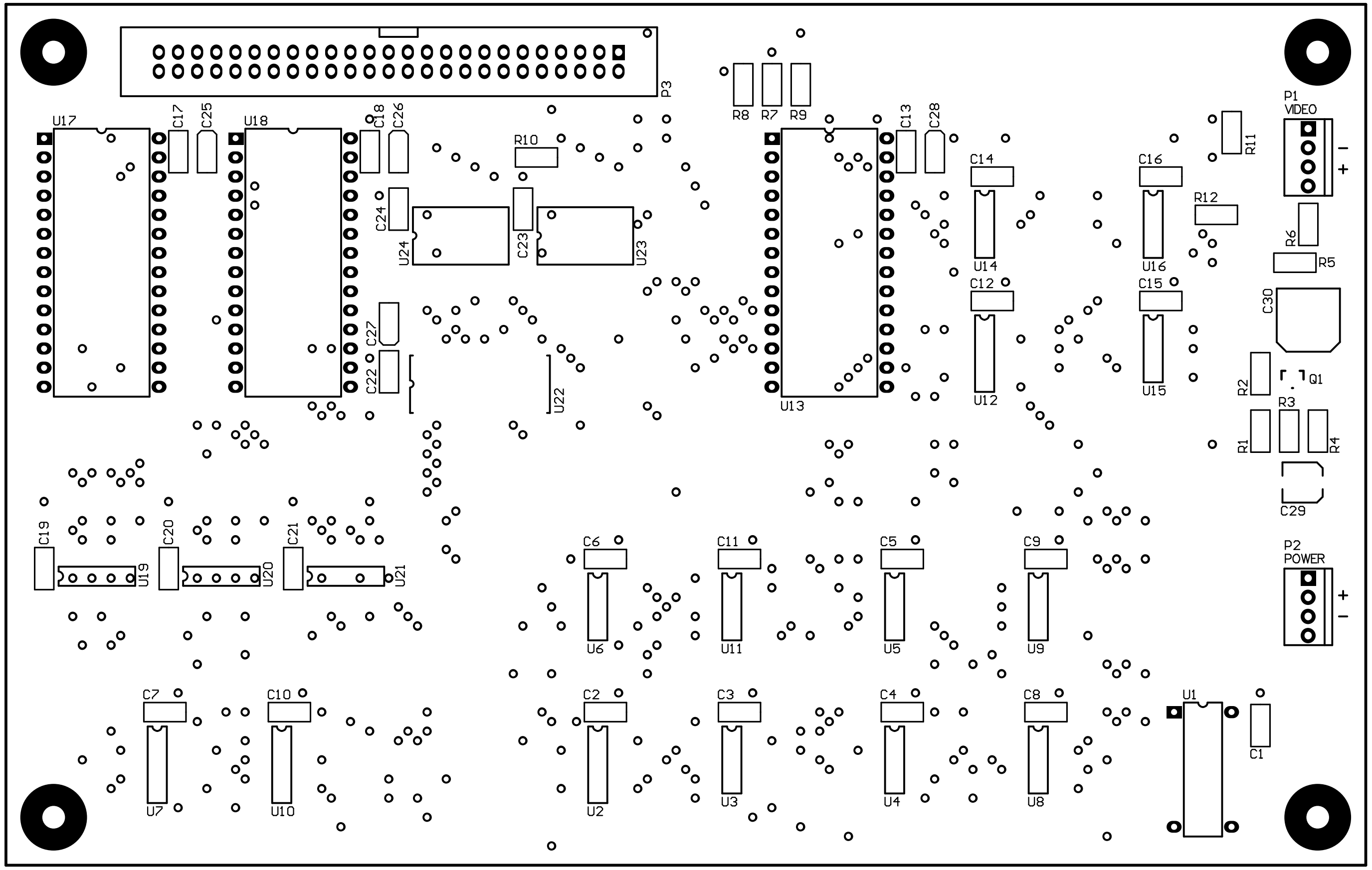


INST DEL
RETURN
SHIFT
OFF RVS
RUN STOP
SPACE
CLR HOME
CRSR

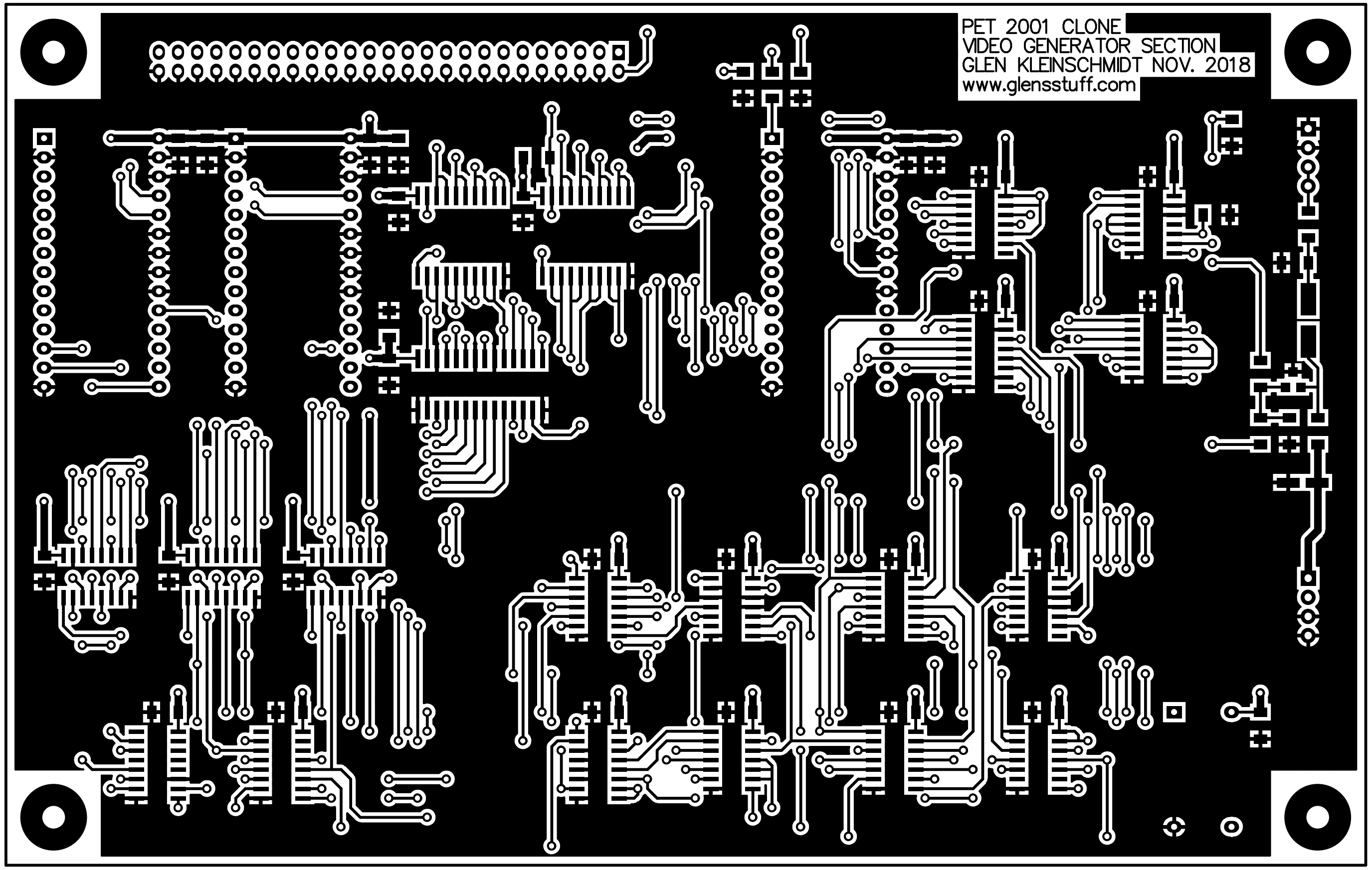

PET-2001 CLONE
GLEN KLEINSCHMIDT AUGUST 2018
POWER
OFF
READ
WRITE
CB2
AUDIO SOURCE
VOLUME
RESET
LEVEL 2
BASIC
LEVEL 3
50 Hz (SYNC)
JIFFY CLOCK
60 Hz
PARALLEL PORT
IEEE-488 PORT
CASSETTE #1
CASSETTE #2
RS-232
INTERFACE
PS/2 KEYBOARD
VIDEO OUT
AUDIO OUT

VIDEO GENERATOR BOARD





P3
U17
C17
C25
U18
C18
C26
R10
R8
R7
R9
C13
C28
C14
C16
R11
P1
VIDEO
−
+
C24
U24
C23
U23
U14
U16
R12
R6
R5
C12
C15
C30
C27
C22
U22
U13
U12
U15
R2
Q1
R3
R1
R4
C29
C19
U19
C20
U20
C21
U21
C6
C11
C5
C9
P2
POWER
+
−
U6
U11
U5
U9
C7
C10
C2
C3
C4
C8
U1
C1
U7
U10
U2
U3
U4
U8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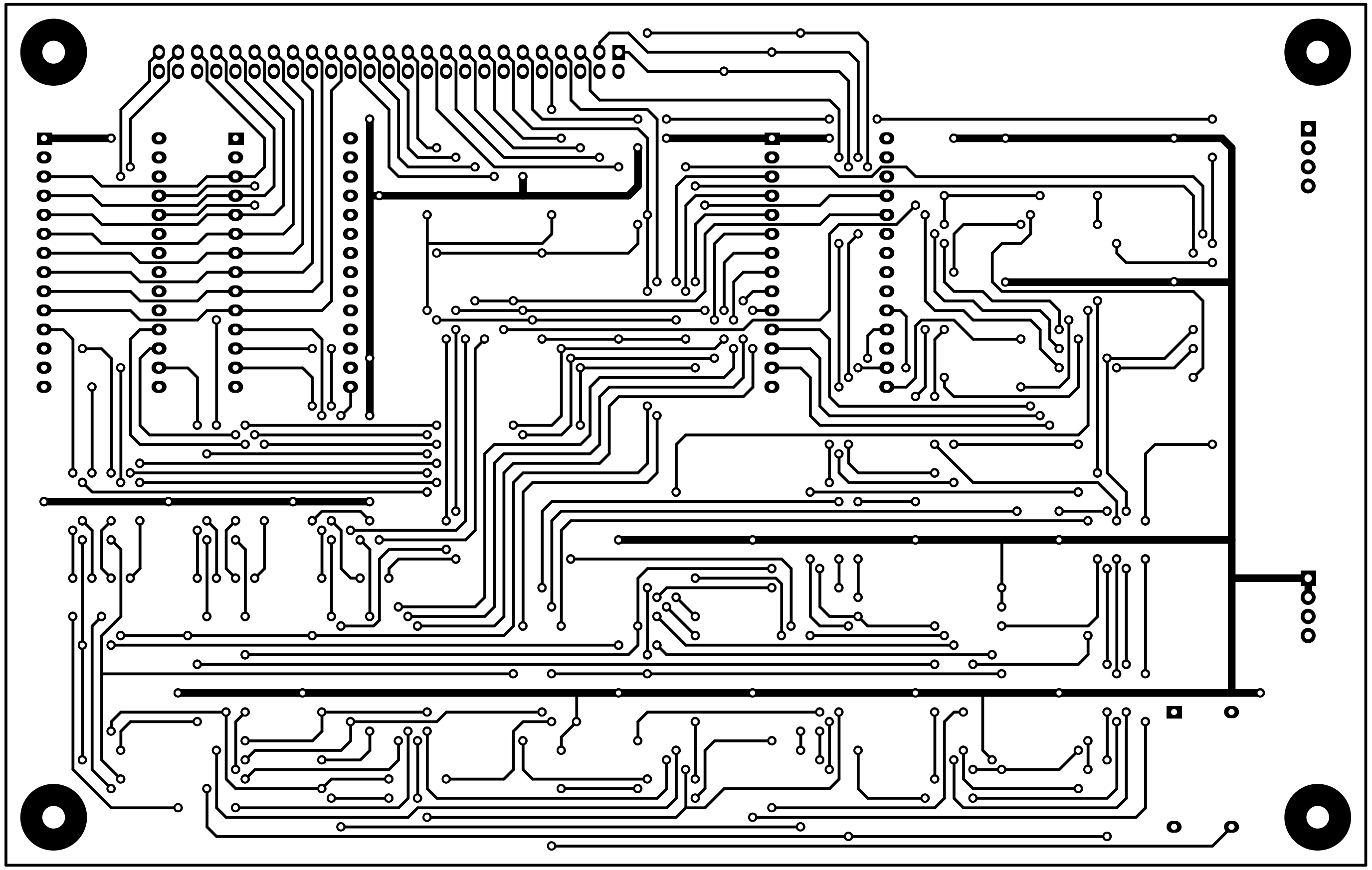
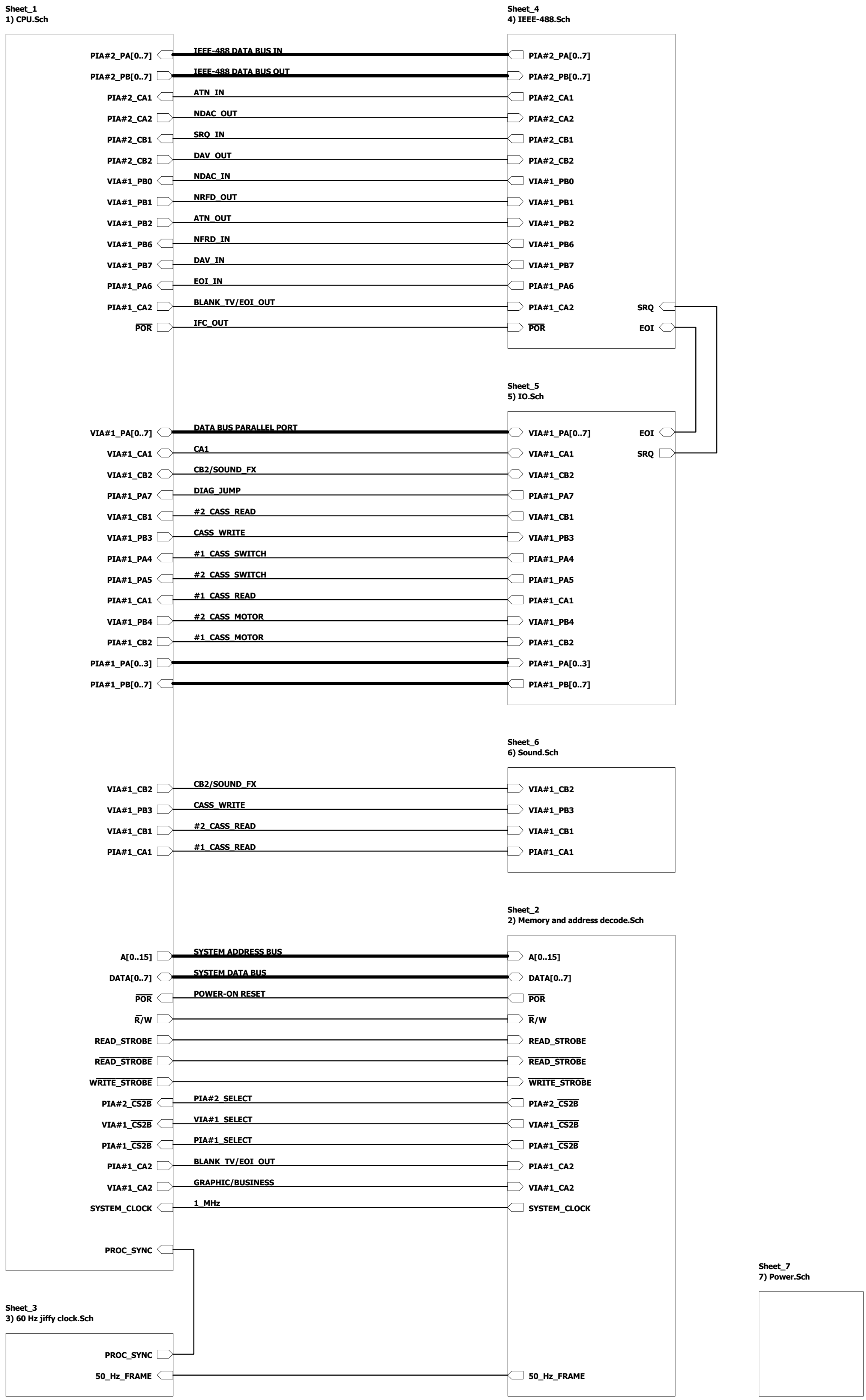
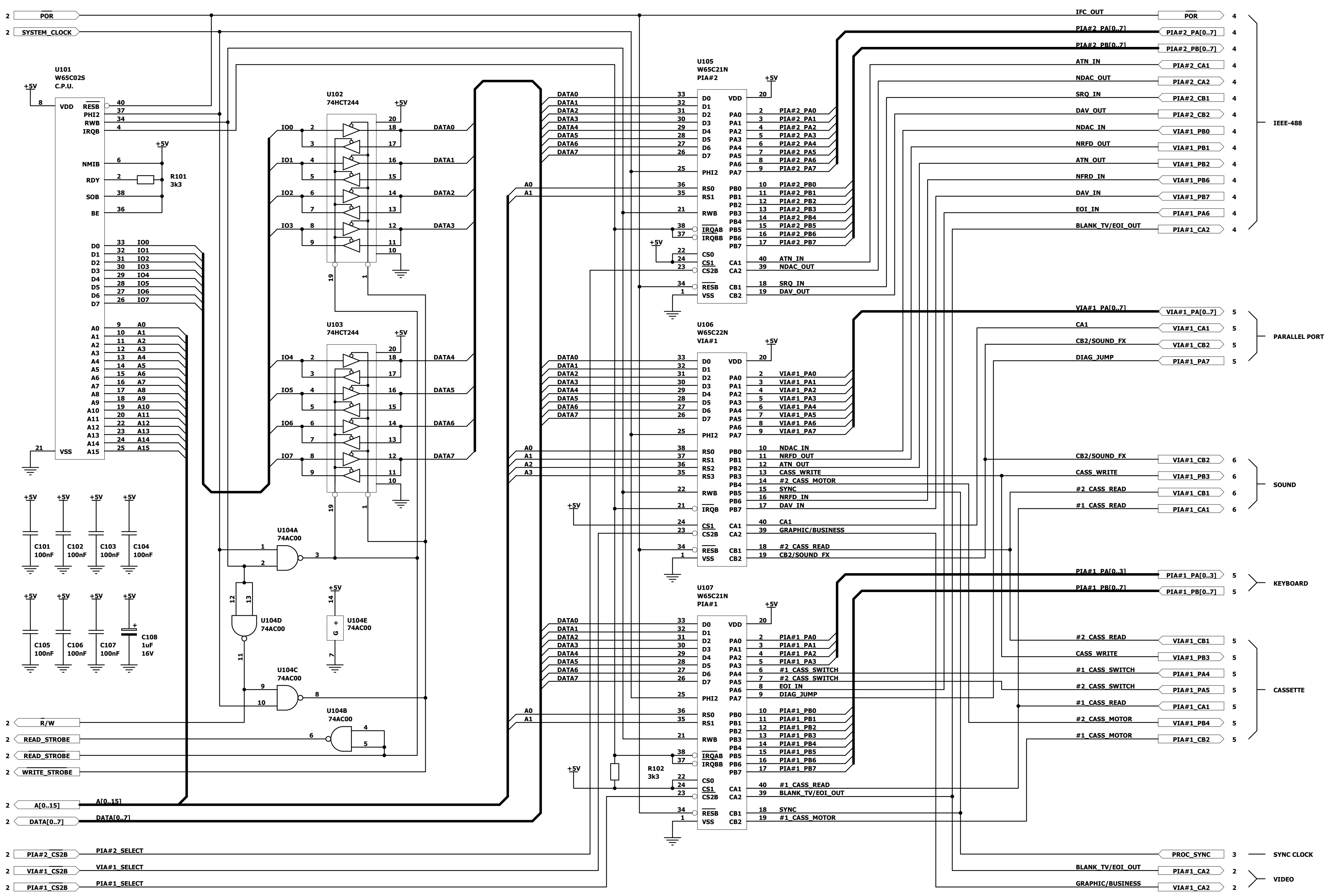


PET 2001 CLONE

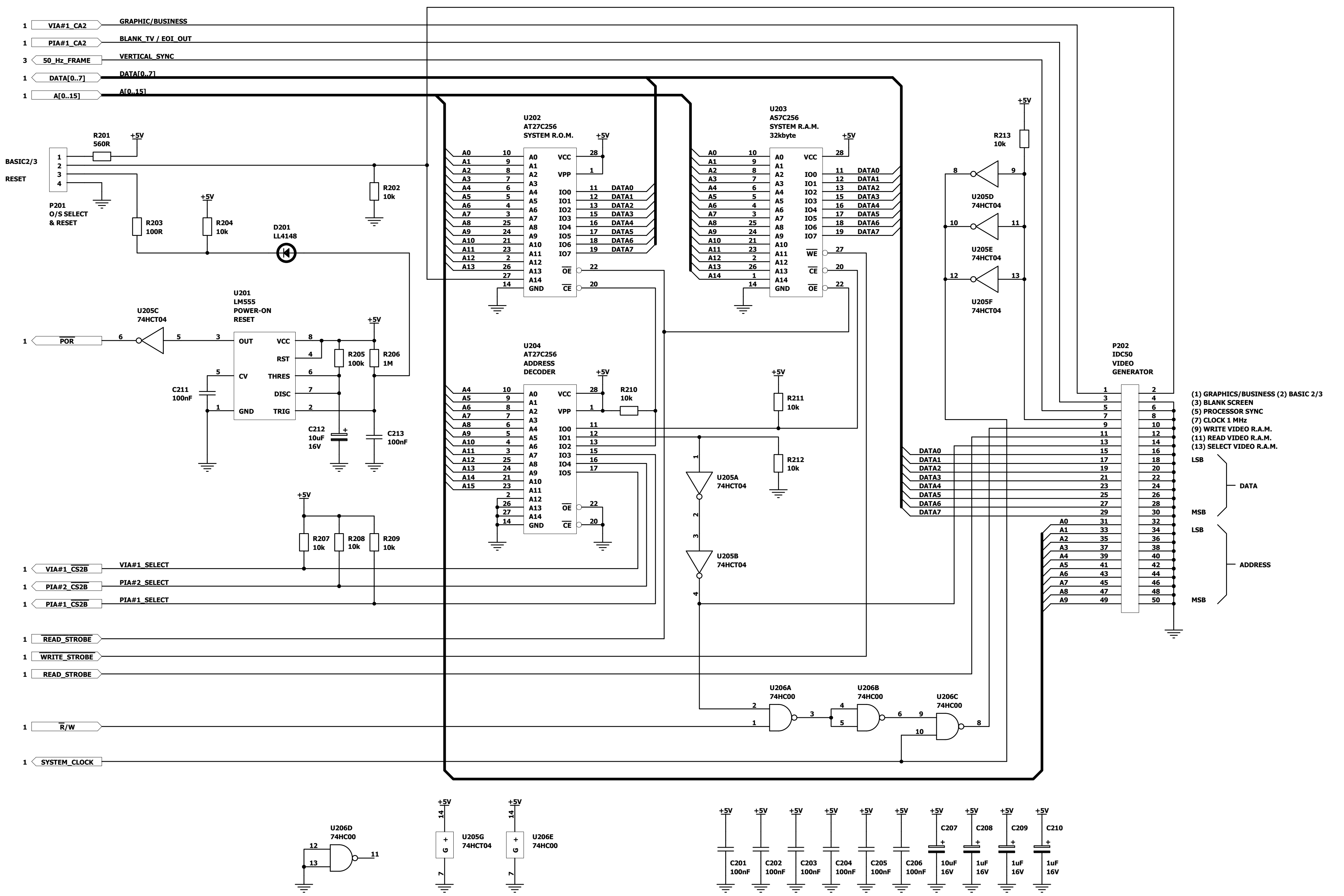


1) CPU

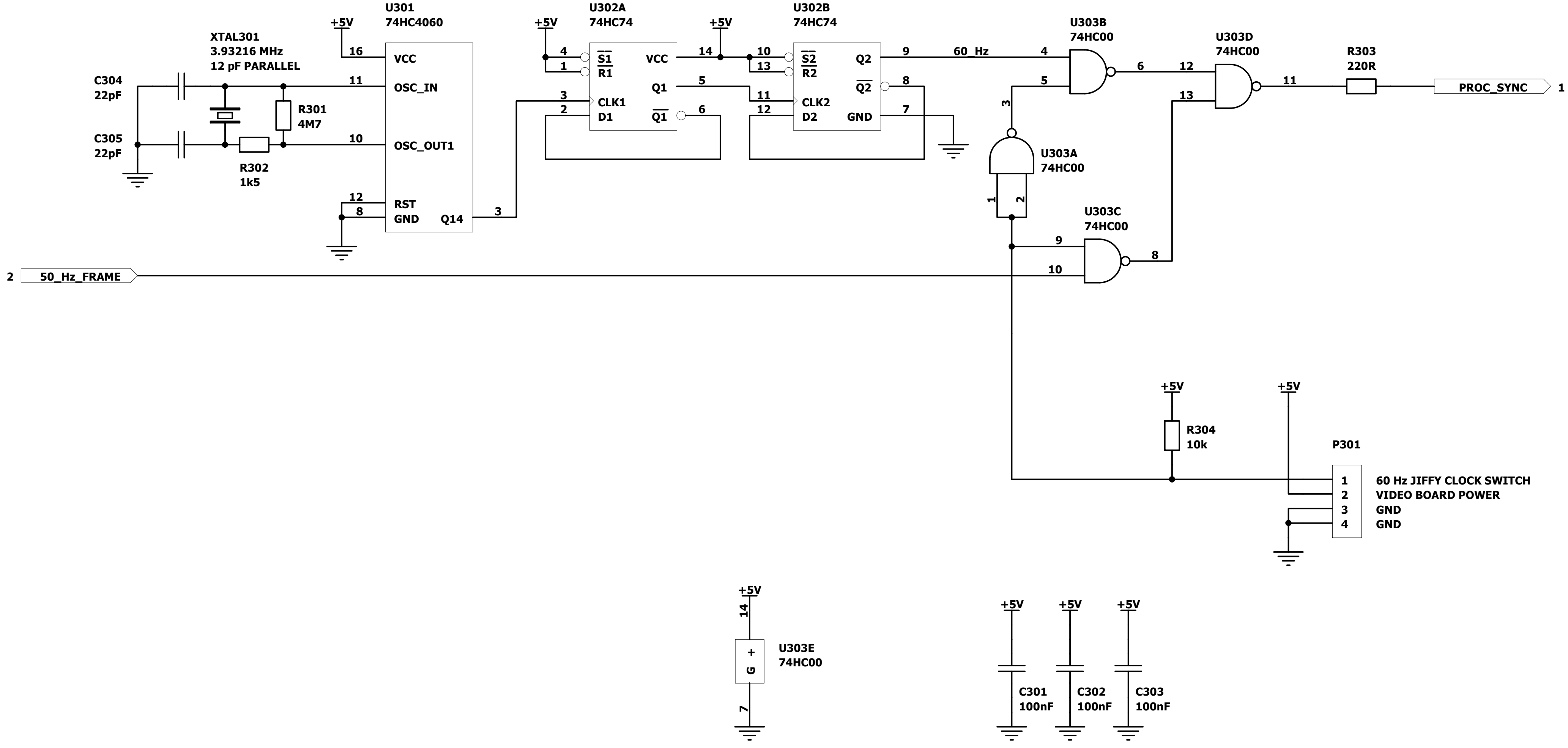


U101
W65C02S
C.P.U.
U102
74HCT244
U103
74HCT244
U104A
74AC00
U104B
74AC00
U104C
74AC00
U104D
74AC00
U104E
74AC00
U105
W65C21N
PIA#2
U106
W65C22N
VIA#1
U107
W65C21N
PIA#1
R101
3k3
R102
3k3
C101 100nF
C102 100nF
C103 100nF
C104 100nF
C105 100nF
C106 100nF
C107 100nF
C108 1uF 16V
POR
SYSTEM_CLOCK
R/W
READ_STROBE
WRITE_STROBE
A[0..15]
DATA[0..7]
PIA#2_CS2B
VIA#1_CS2B
PIA#1_CS2B
PIA#2_SELECT
VIA#1_SELECT
PIA#1_SELECT
IFC_OUT
PIA#2_PA[0..7]
PIA#2_PB[0..7]
ATN_IN
NDAC_OUT
SRQ_IN
DAV_OUT
NDAC_IN
NRFD_OUT
ATN_OUT
NFRD_IN
DAV_IN
EOI_IN
BLANK_TV/EOI_OUT
IEEE-488
VIA#1_PA[0..7]
CA1
CB2/SOUND_FX
DIAG_JUMP
PARALLEL PORT
CASS_WRITE
#2_CASS_READ
#1_CASS_READ
SOUND
PIA#1_PA[0..3]
PIA#1_PB[0..7]
KEYBOARD
#1_CASS_SWITCH
#2_CASS_SWITCH
#2_CASS_MOTOR
#1_CASS_MOTOR
CASSETTE
PROC_SYNC
SYNC CLOCK
GRAPHIC/BUSINESS
VIDEO

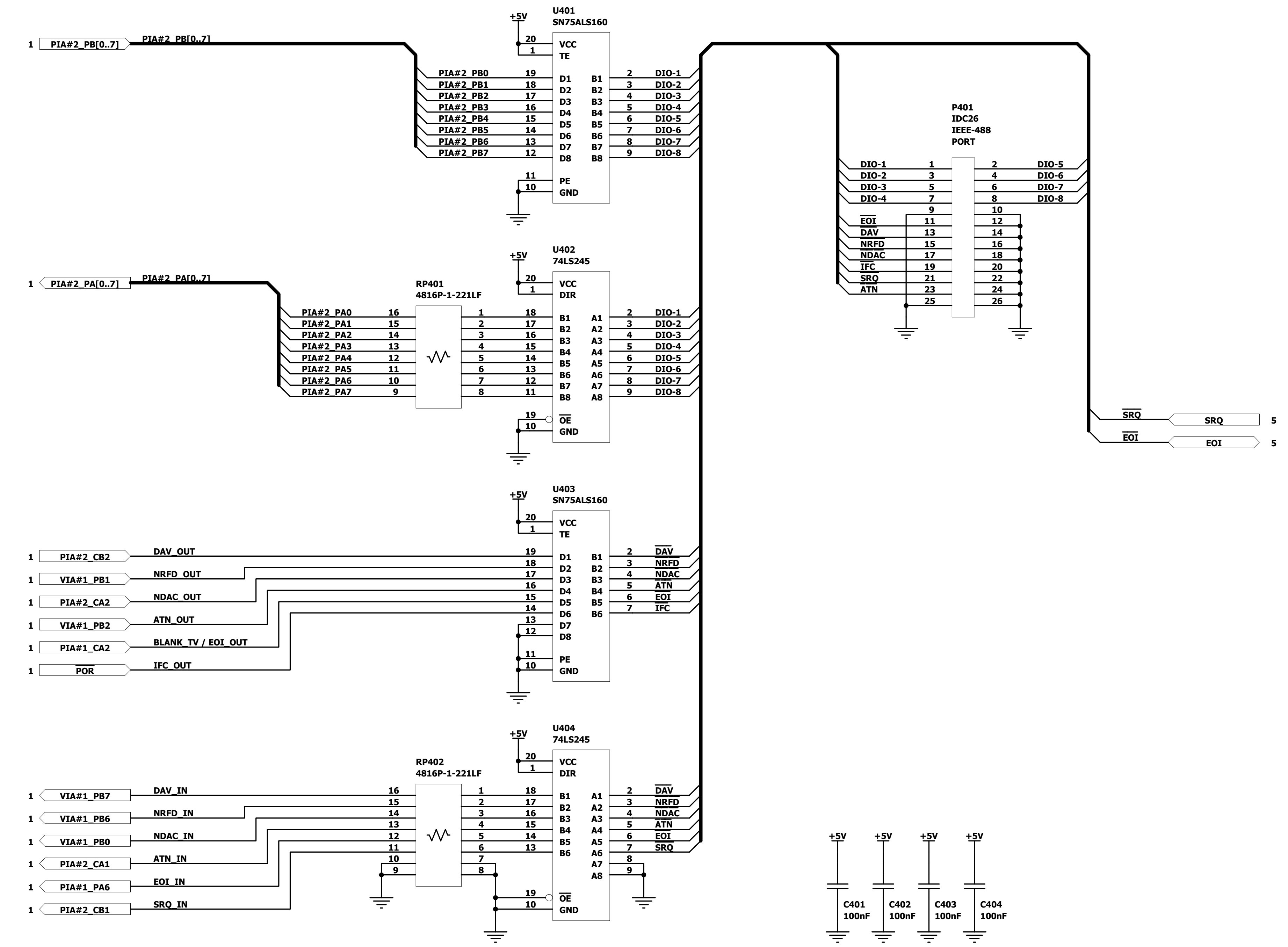
2) MEMORY AND ADDRESS DECODE



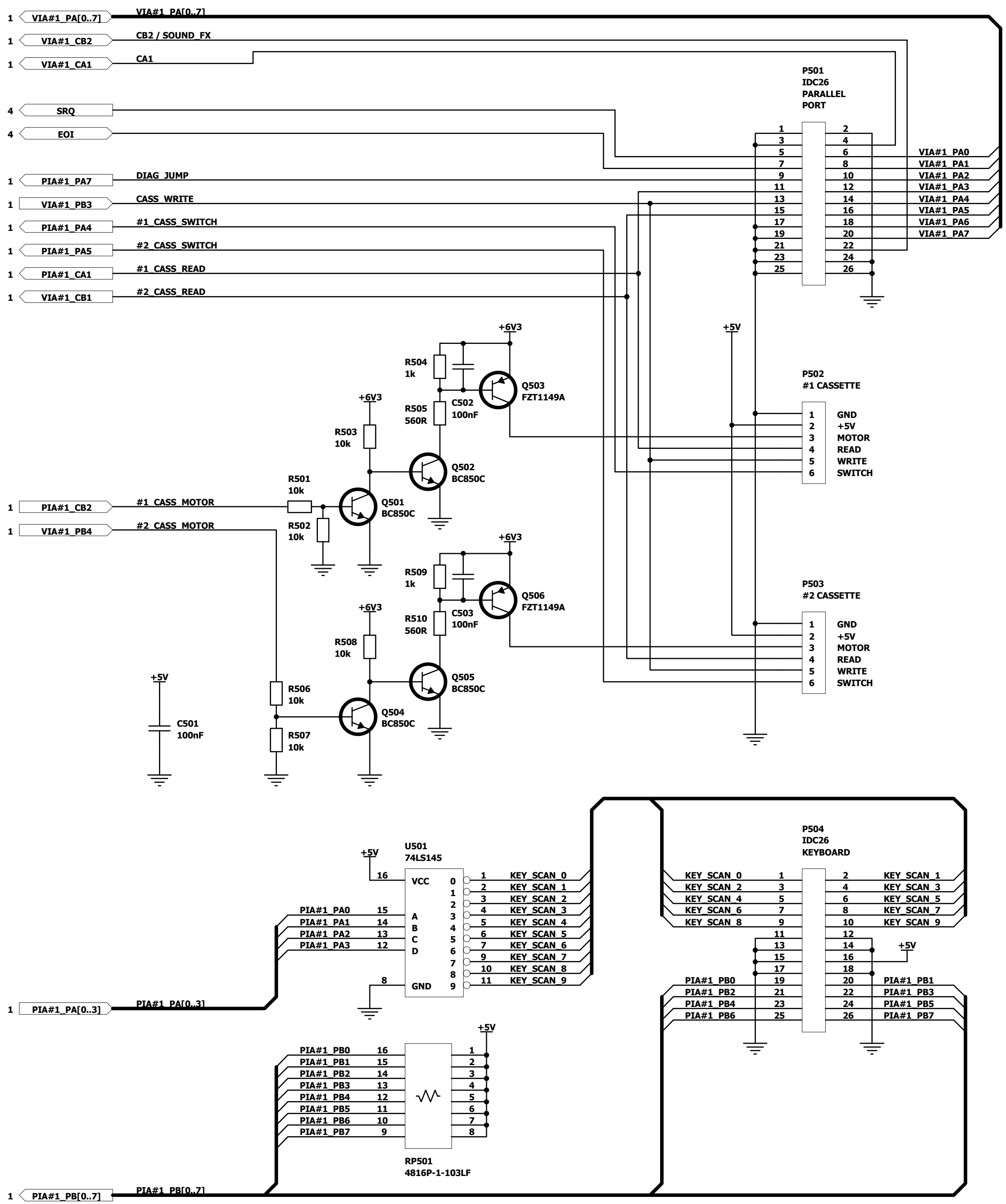
3) 60 Hz JIFFY CLOCK



4) IEEE-488 INTERFACE PORT

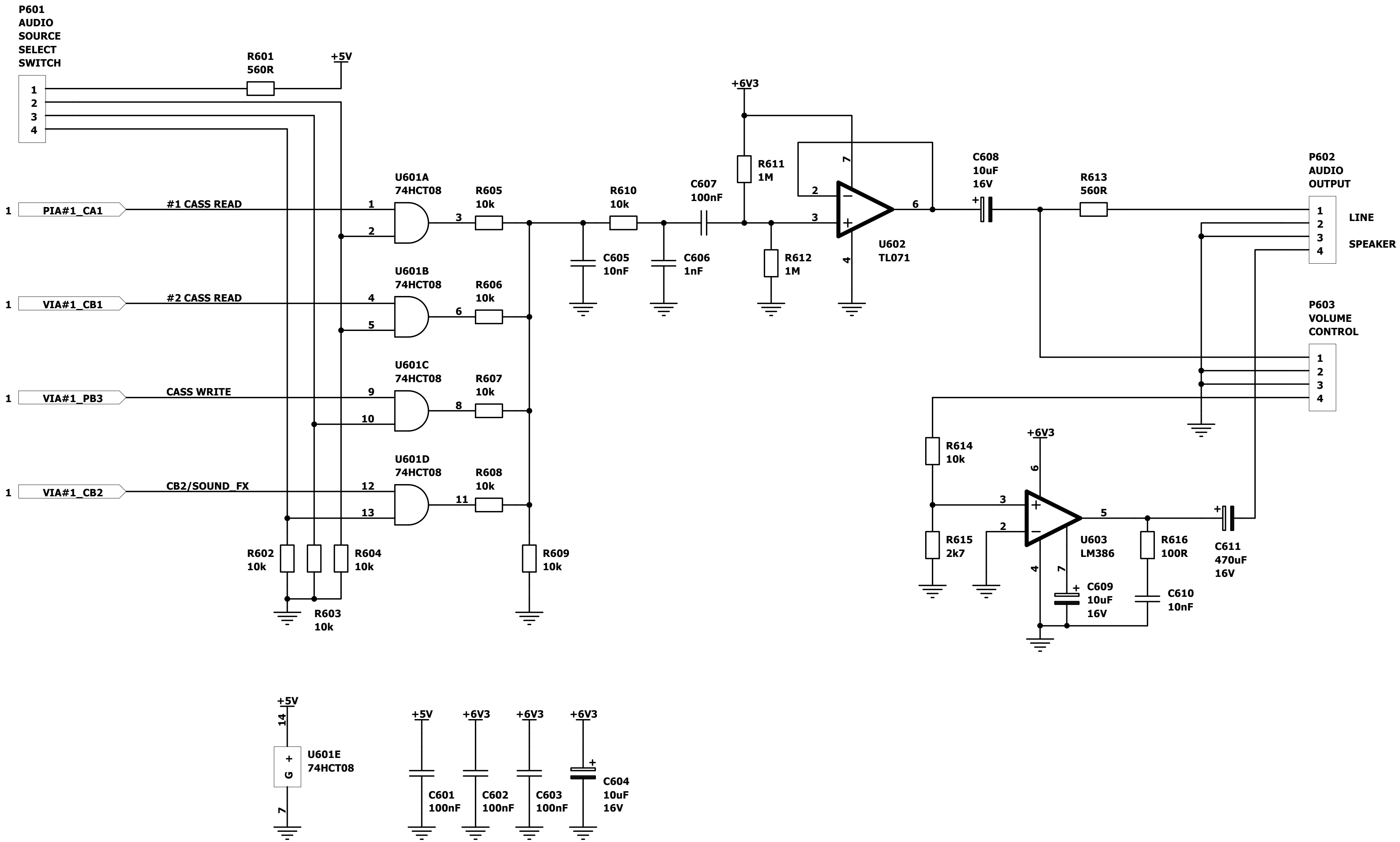


5) I/O



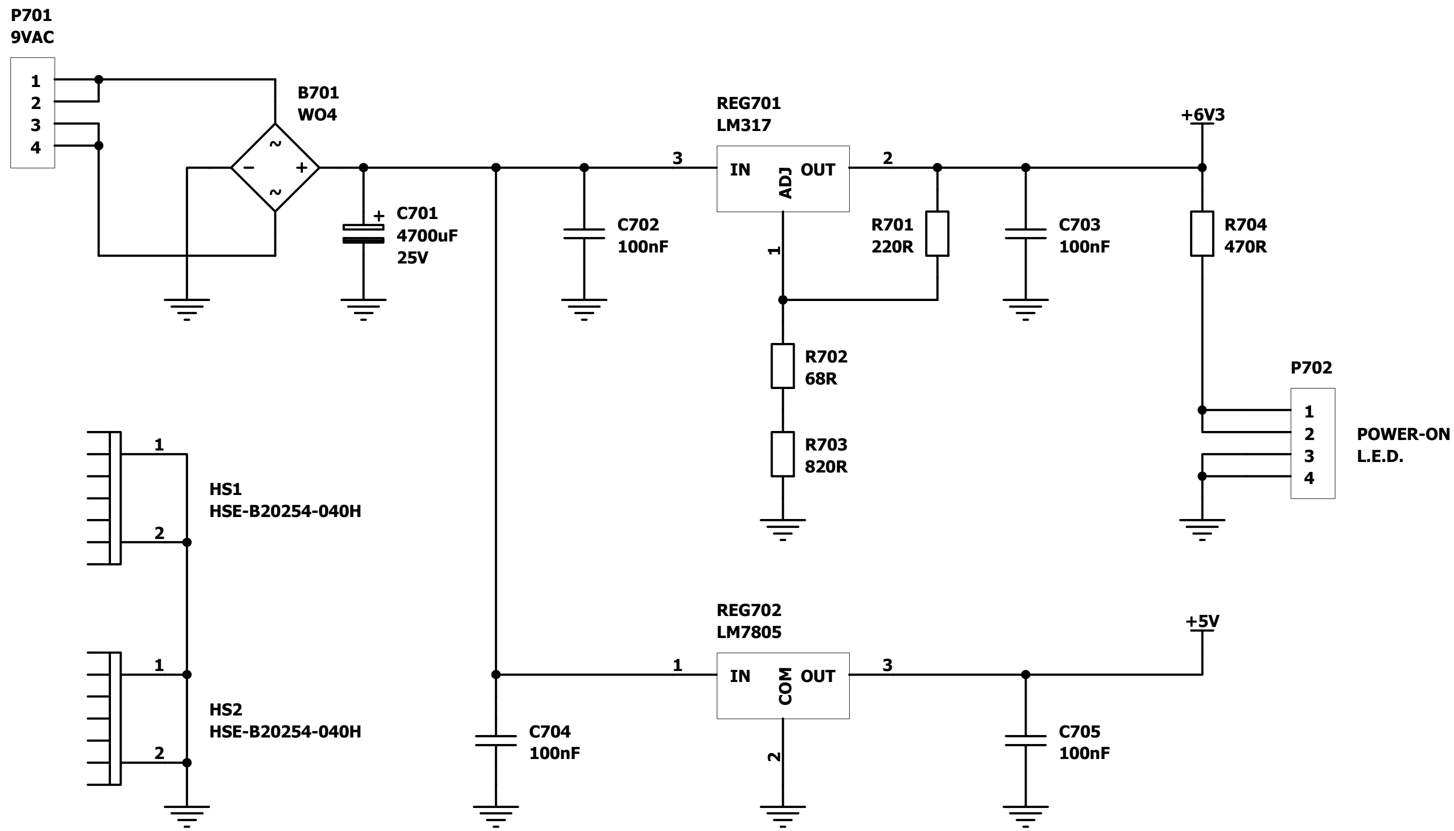
VIA#1_PA[0..7]
VIA#1_CB2
VIA#1_CA1
SRQ
EOI
PIA#1_PA7
VIA#1_PB3
PIA#1_PA4
PIA#1_PA5
PIA#1_CA1
VIA#1_CB1
CB2 / SOUND_FX
CA1
DIAG_JUMP
CASS_WRITE
#1_CASS_SWITCH
#2_CASS_SWITCH
#1_CASS_READ
#2_CASS_READ
P501 IDC26 PARALLEL PORT
VIA#1_PA0
VIA#1_PA1
VIA#1_PA2
VIA#1_PA3
VIA#1_PA4
VIA#1_PA5
VIA#1_PA6
VIA#1_PA7
P502 #1 CASSETTE
P503 #2 CASSETTE
GND
+5V
MOTOR
READ
WRITE
SWITCH
+6V3
R504 1k
R505 560R
C502 100nF
Q503 FZT1149A
R503 10k
Q502 BC850C
R501 10k
R502 10k
Q501 BC850C
VIA#1_CB2
VIA#1_PB4
#1_CASS_MOTOR
#2_CASS_MOTOR
R509 1k
R510 560R
C503 100nF
Q506 FZT1149A
R508 10k
Q505 BC850C
R506 10k
R507 10k
Q504 BC850C
C501 100nF
U501 74LS145
VCC
GND
PIA#1_PA0
PIA#1_PA1
PIA#1_PA2
PIA#1_PA3
PIA#1_PA[0..3]
KEY_SCAN_0
KEY_SCAN_1
KEY_SCAN_2
KEY_SCAN_3
KEY_SCAN_4
KEY_SCAN_5
KEY_SCAN_6
KEY_SCAN_7
KEY_SCAN_8
KEY_SCAN_9
P504 IDC26 KEYBOARD
PIA#1_PB0
PIA#1_PB1
PIA#1_PB2
PIA#1_PB3
PIA#1_PB4
PIA#1_PB5
PIA#1_PB6
PIA#1_PB7
RP501 4816P-1-103LF
PIA#1_PB[0..7]

6) SOUND

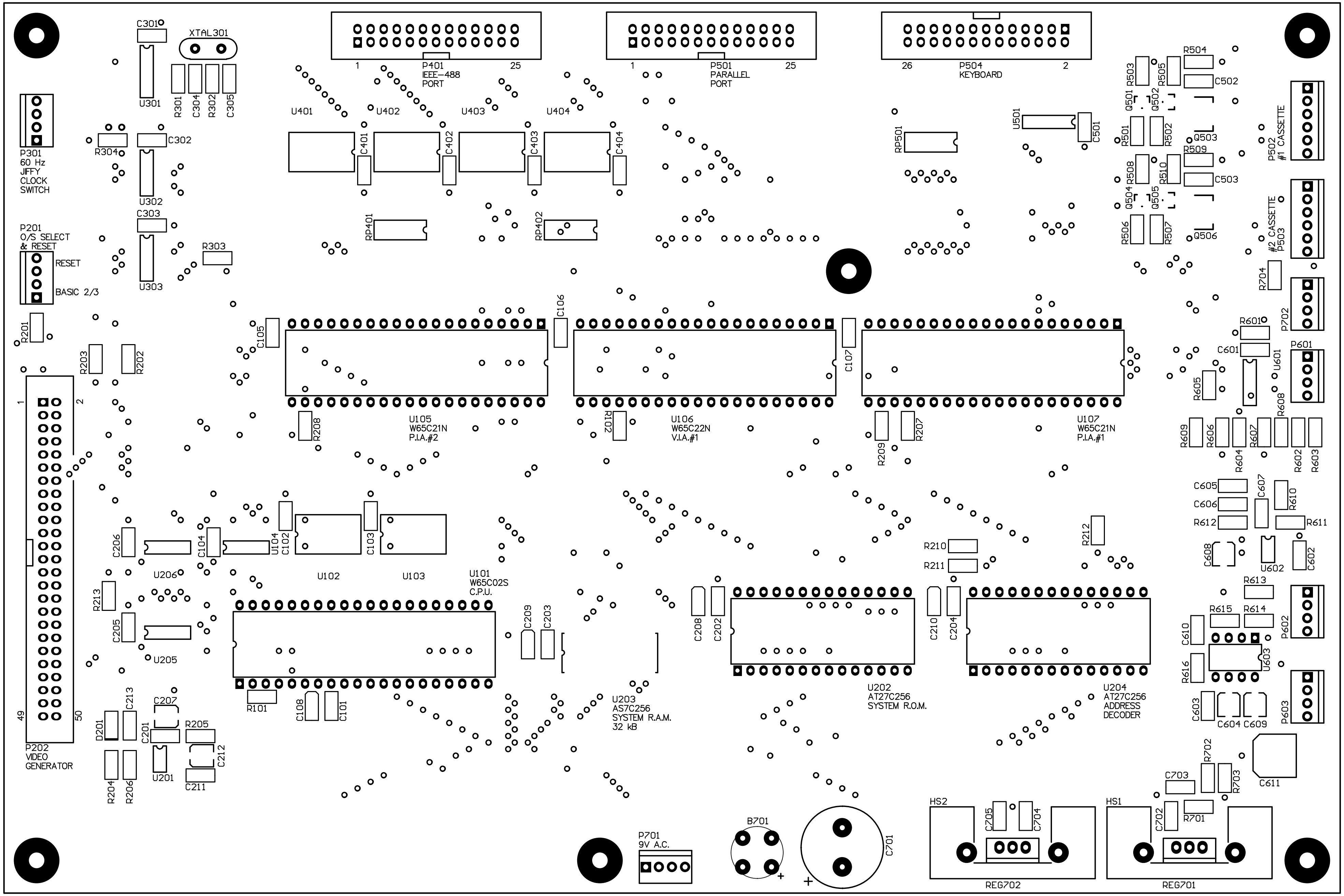


P601 AUDIO SOURCE SELECT SWITCH
R601 560R
+5V
PIA#1_CA1
#1 CASS READ
VIA#1_CB1
#2 CASS READ
VIA#1_PB3
CASS WRITE
VIA#1_CB2
CB2/SOUND_FX
U601A 74HCT08
U601B 74HCT08
U601C 74HCT08
U601D 74HCT08
R605 10k
R606 10k
R607 10k
R608 10k
R602 10k
R603 10k
R604 10k
R609 10k
R610 10k
C605 10nF
C606 1nF
C607 100nF
+6V3
R611 1M
R612 1M
U602 TL071
C608 10uF 16V
R613 560R
P602 AUDIO OUTPUT
LINE
SPEAKER
P603 VOLUME CONTROL
R614 10k
R615 2k7
U603 LM386
R616 100R
C609 10uF 16V
C610 10nF
C611 470uF 16V
U601E 74HCT08
C601 100nF
C602 100nF
C603 100nF
C604 10uF 16V

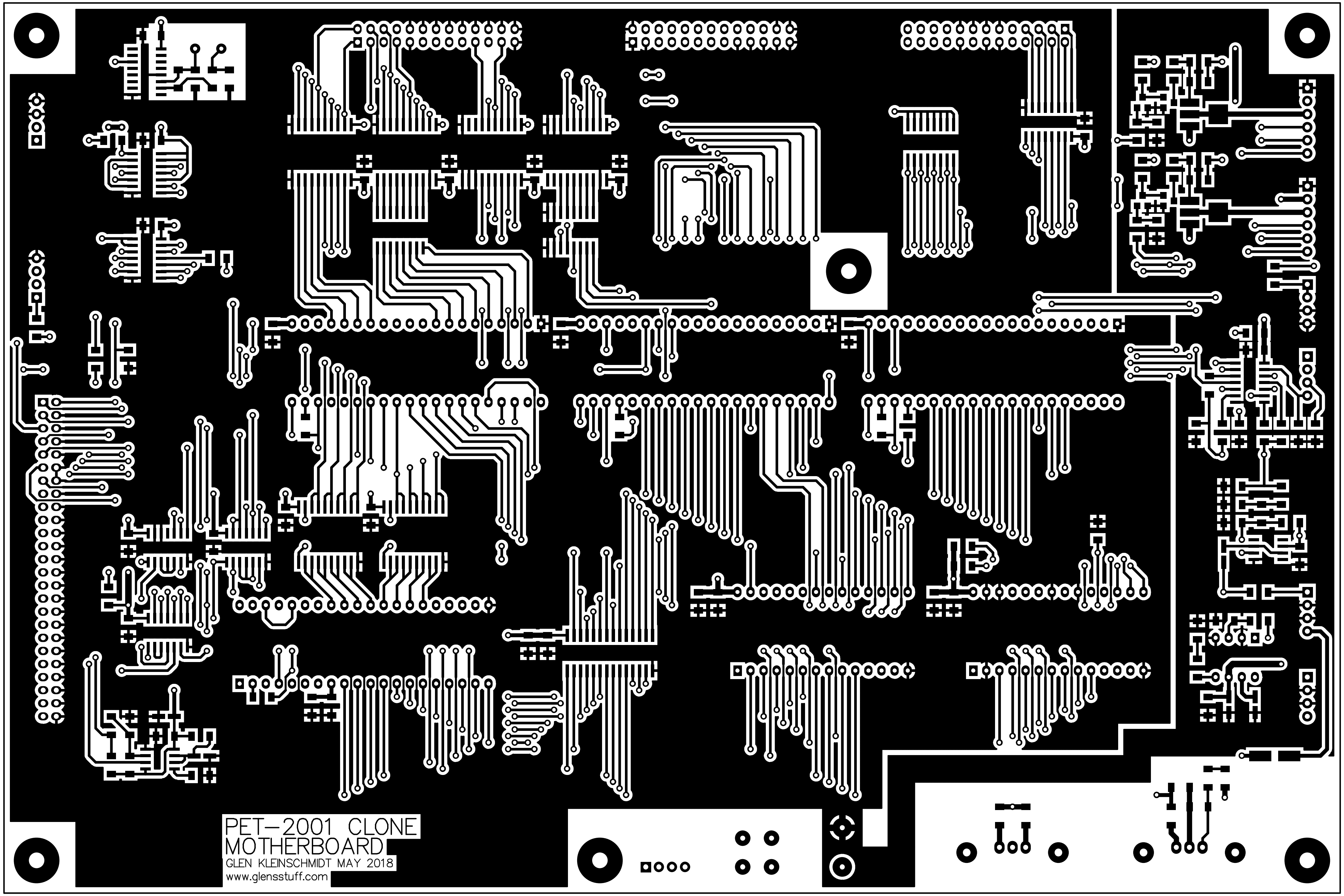
7) POWER

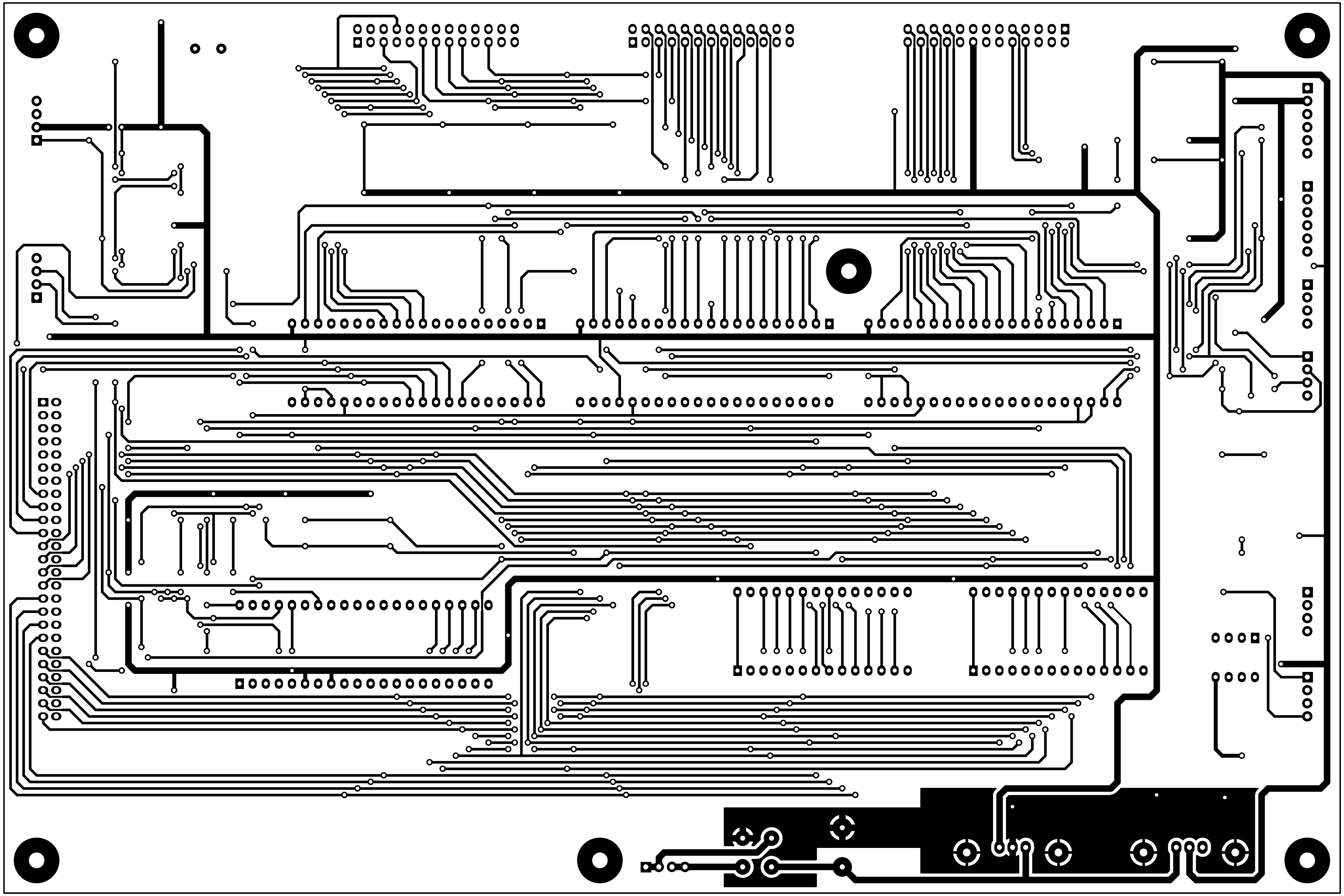


P701
9VAC
1
2
3
4
B701
WO4
C701
4700uF
25V
C702
100nF
REG701
LM317
IN
ADJ
OUT
3
2
1
R701
220R
C703
100nF
+6V3
R704
470R
R702
68R
R703
820R
P702
1
2
3
4
POWER-ON
L.E.D.
HS1
HSE-B20254-040H
HS2
HSE-B20254-040H
REG702
LM7805
IN
COM
OUT
1
3
2
+5V
C704
100nF
C705
100nF

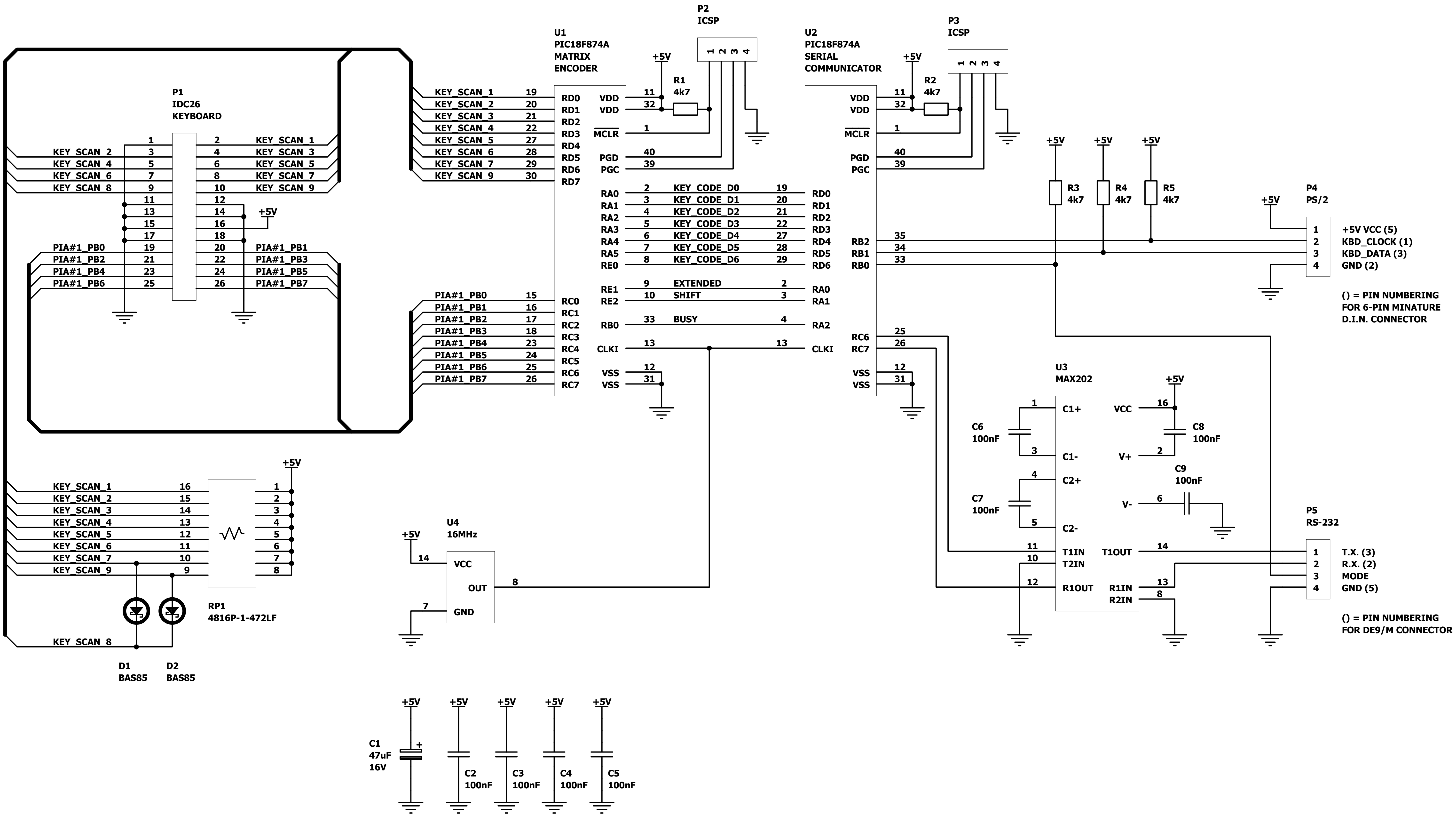


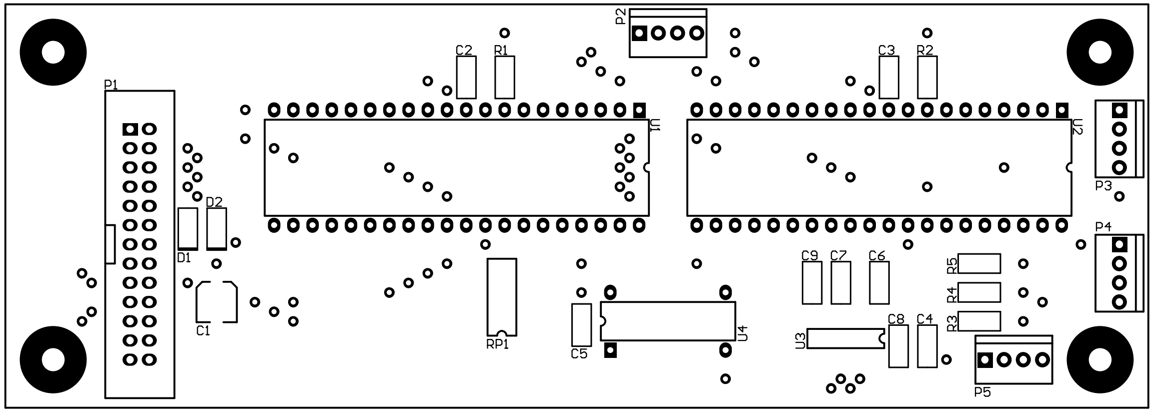
C301
XTAL301
U301
R301
C304
R302
C305
P401
IEEE-488
PORT
P501
PARALLEL
PORT
P504
KEYBOARD
R504
R503
R505
C502
Q501
Q502
P502
#1 CASSETTE
P301
60 Hz
JIFFY
CLOCK
SWITCH
R304
C302
U302
U401
U402
U403
U404
C401
C402
C403
C404
RP401
RP402
RP501
U501
C501
R501
R502
Q503
R509
R508
R510
C503
Q504
Q505
Q506
R506
R507
#2 CASSETTE
P503
P201
O/S SELECT
& RESET
RESET
BASIC 2/3
C303
U303
R303
R704
P702
R201
C105
C106
C107
R601
C601
U601
P601
R203
R202
R605
R608
R208
U105
W65C21N
P.I.A.#2
R102
U106
W65C22N
V.I.A.#1
R209
R207
U107
W65C21N
P.I.A.#1
R609
R606
R604
R607
R602
R603
P202
VIDEO
GENERATOR
C605
C606
C607
R610
R612
R611
C206
U206
C104
U104
C102
U102
C103
U103
U101
W65C02S
C.P.U.
R210
R211
R212
C608
U602
C602
R213
C205
U205
C209
C203
C208
C202
C210
C204
R613
R615
R614
P602
C610
U603
R616
R101
C108
C101
U203
AS7C256
SYSTEM R.A.M.
32 kB
U202
AT27C256
SYSTEM R.O.M.
U204
AT27C256
ADDRESS
DECODER
C603
C604
C609
P603
D201
C213
C207
C201
R205
C212
U201
C211
R204
R206
R702
R703
C611
C703
P701
9V A.C.
B701
C701
HS2
C205
C704
REG702
HS1
C702
R701
REG701

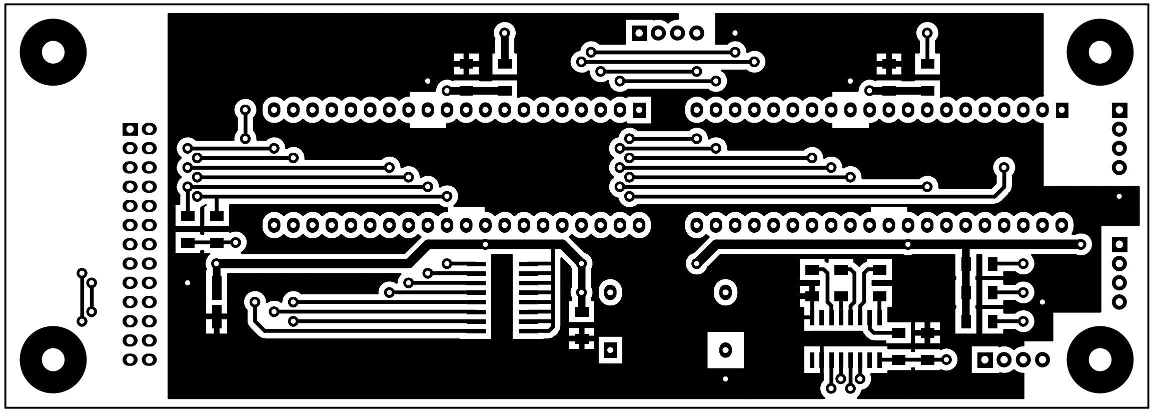

PET-2001 CLONE
MOTHERBOARD
GLEN KLEINSCHMIDT MAY 2018
www.glensstuff.com

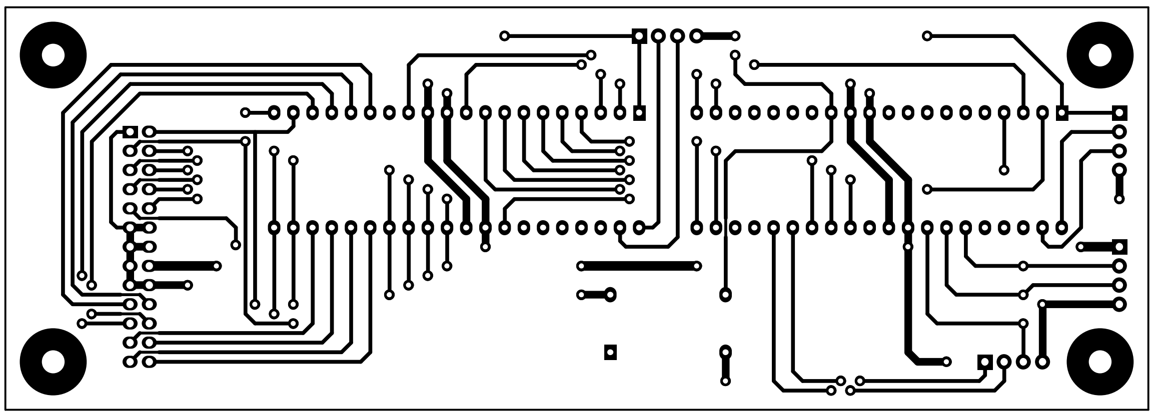


PS/2 KEYBOARD AND RS-232 INTERFACE BOARD

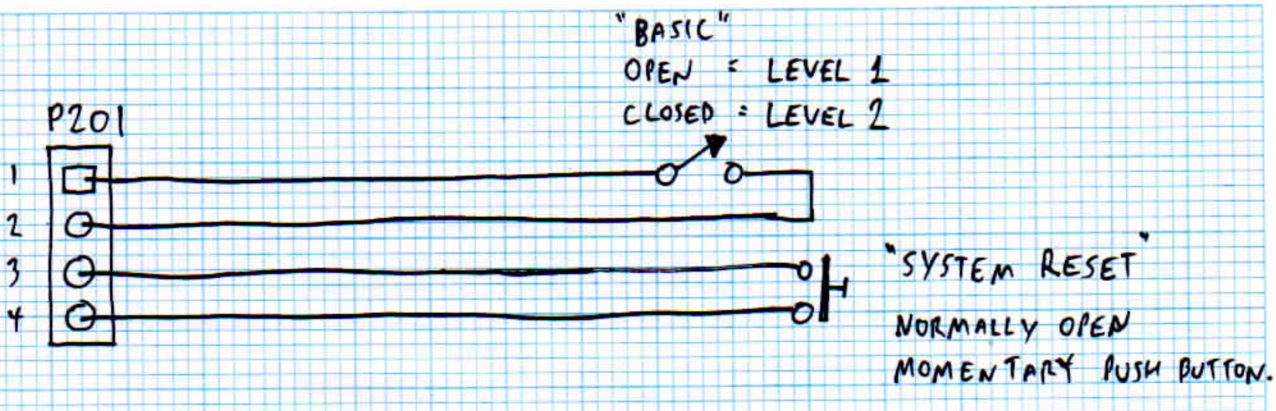


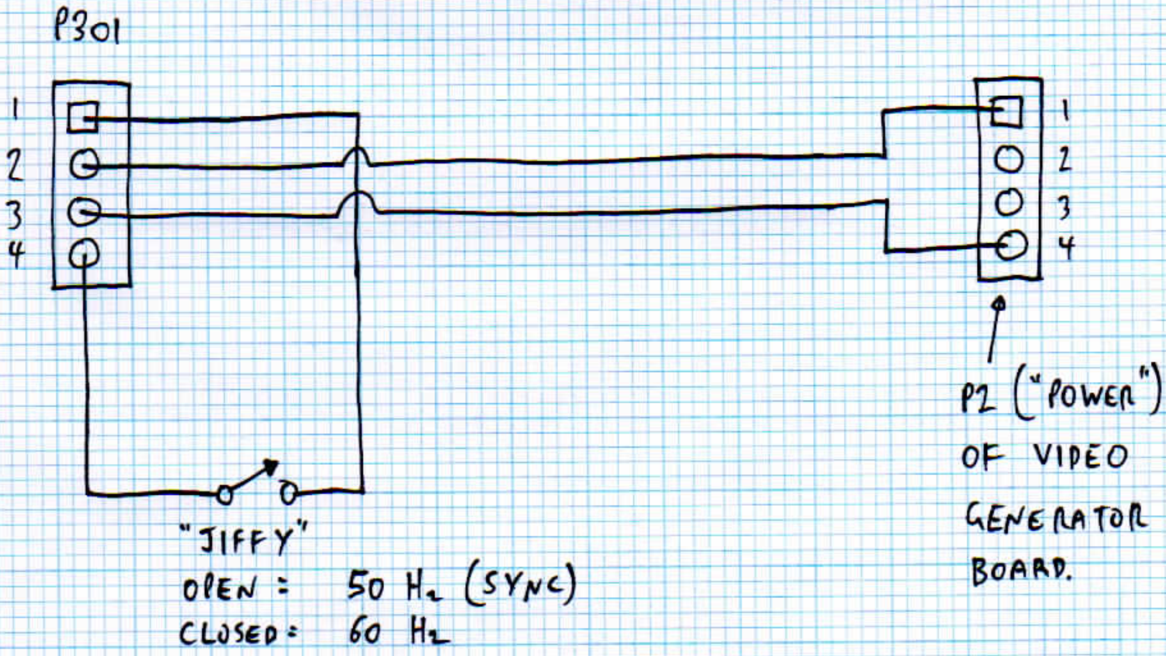

P2
C2
R1
C3
R2
P1
U1
U2
P3
P4
D2
D1
C1
RP1
C5
U4
C9
C7
C6
R5
R4
R3
C8
C4
U3
P5

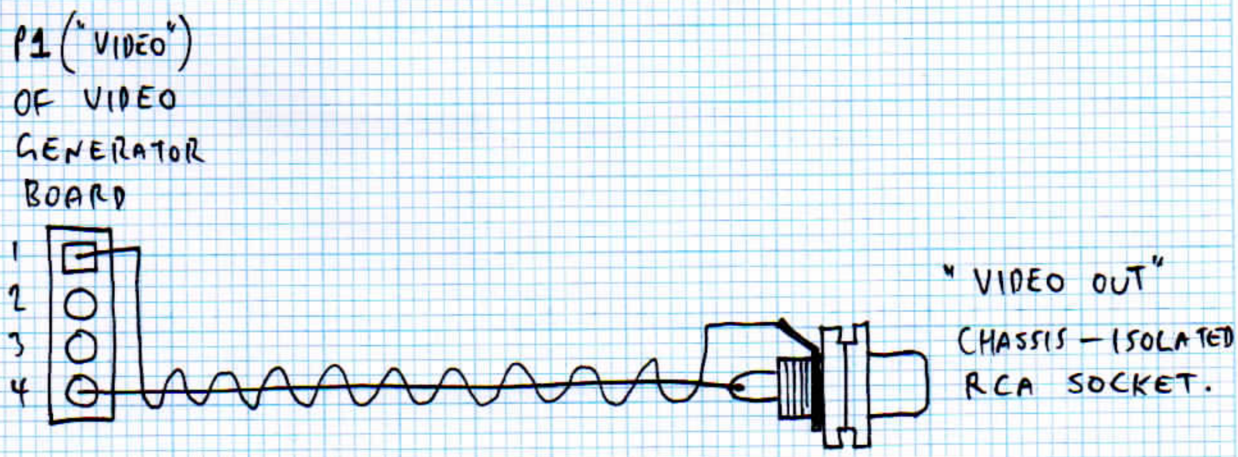




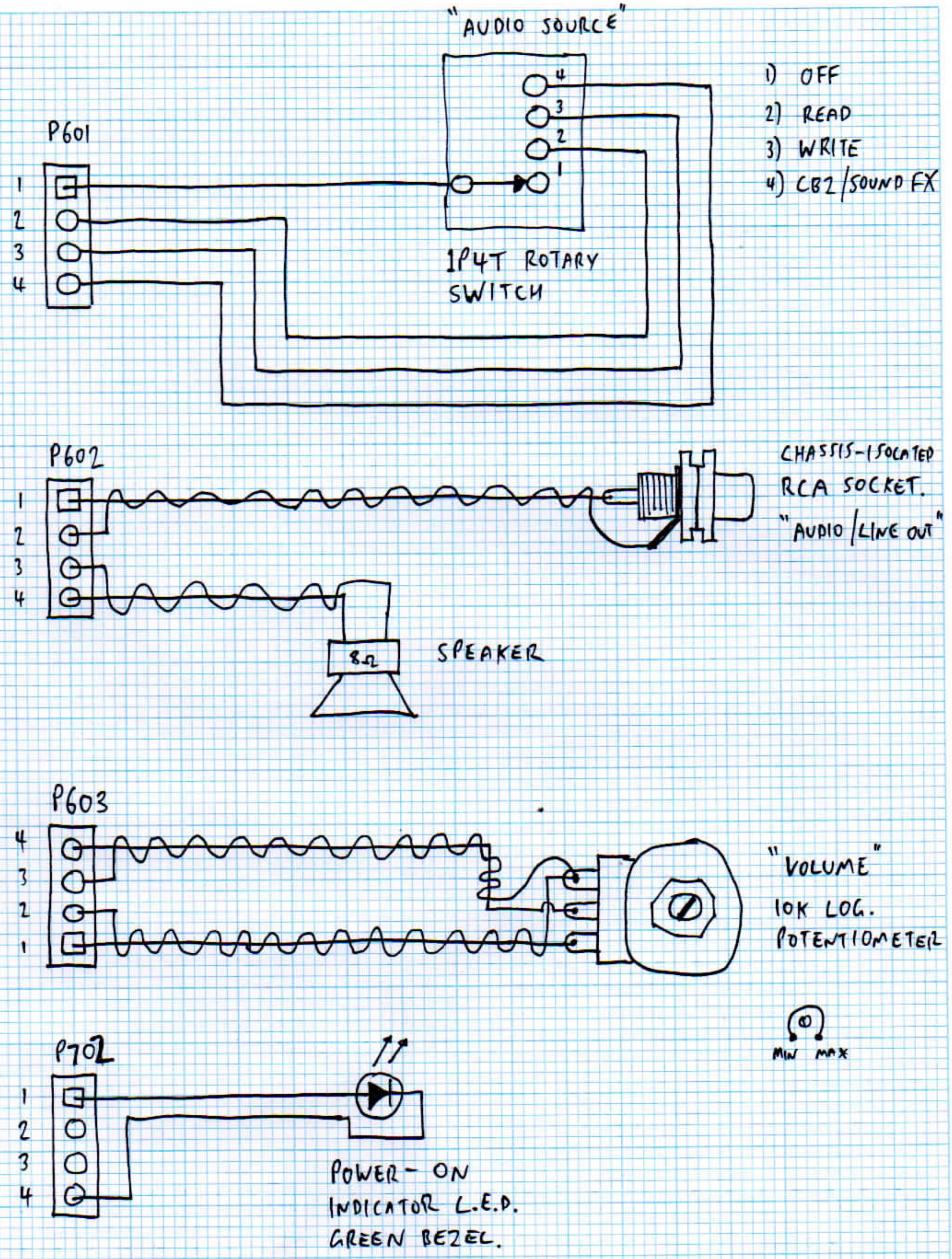
MOTHERBOARD WIRING.

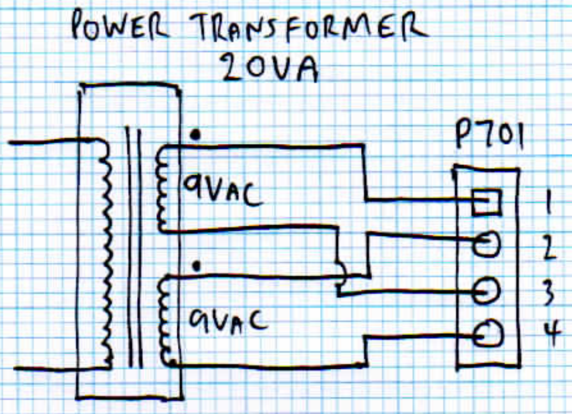


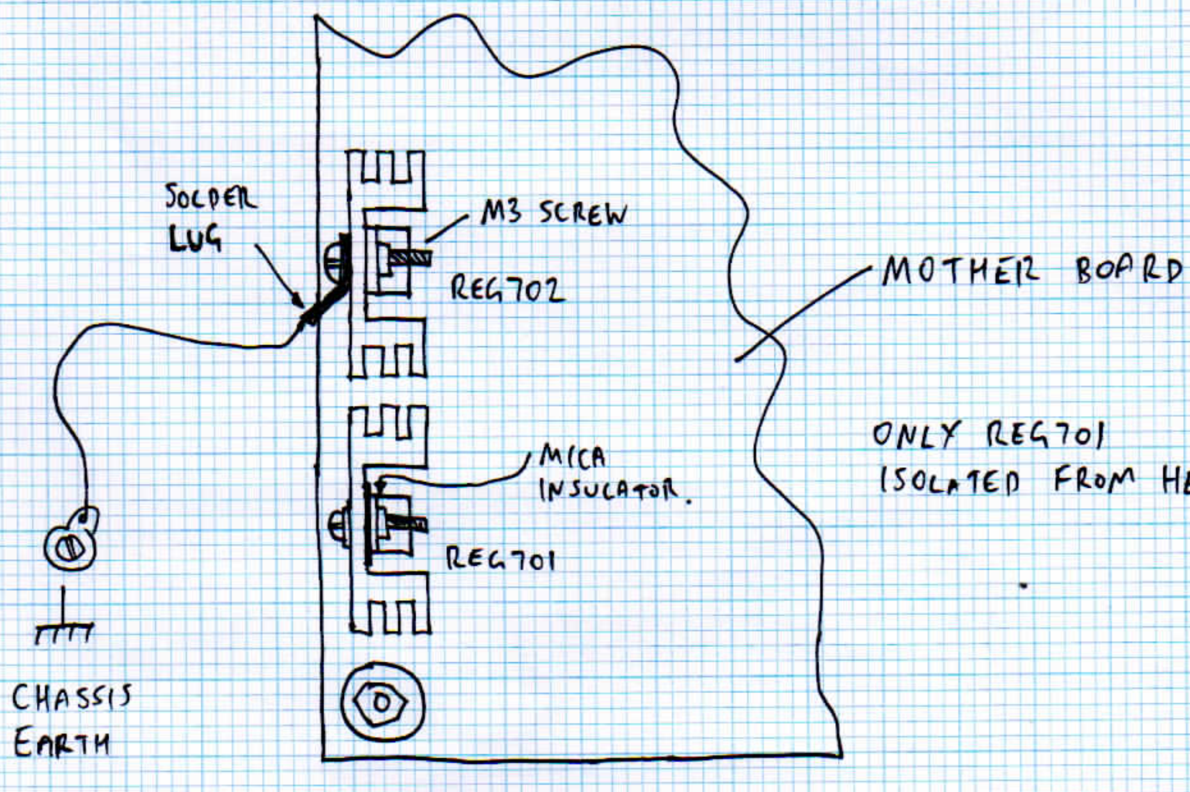




P202 ON MOTHERBOARD CONNECTS TO P3 ON VIDEO GENERATOR BOARD VIA 50-WAY RIBBON CABLE.


"AUDIO SOURCE"
P601
1P4T ROTARY SWITCH
1) OFF
2) READ
3) WRITE
4) CB2/SOUND FX
P602
CHASSIS-ISOLATED RCA SOCKET.
"AUDIO/LINE OUT"
8Ω
SPEAKER
P603
"VOLUME"
10K LOG.
POTENTIOMETER
MIN MAX
P702
POWER-ON
INDICATOR L.E.D.
GREEN BEZEL.





ONLY REG701
ISOLATED FROM HEATSINK.

Parts for Motherboard PCB

Designator	Component type	Value	Part #	Manufacturer	Package	Description	Quantity
R206, R611, R612	Resistor	1M		Various	1206	Chip, thin film	3
R302	Resistor	1k5		Various	1206	Chip, thin film	1
R504, R509	Resistor	1k		Various	1206	Chip, thin film	2
R102, R102	Resistor	3k3		Various	1206	Chip, thin film	2
R301	Resistor	4M7		Various	1206	Chip, thin film	1
R202, R204, R207, R208, R209, R210, R211, R212, R213, R304, R501, R502, R503, R506, R507, R508, R602, R603, R604, R605, R606, R607, R608, R609, R610, R614	Resistor	10k		Various	1206	Chip, thin film	26
R615	Resistor	2k7		Various	1206	Chip, thin film	1
R702	Resistor	68R		Various	1206	Chip, thin film	1
R203, R616	Resistor	100R		Various	1206	Chip, thin film	2
R205	Resistor	100k		Various	1206	Chip, thin film	1
R303, R701	Resistor	220R		Various	1206	Chip, thin film	2
R704	Resistor	470R		Various	1206	Chip, thin film	1
R201, R505, R510, R601, R613	Resistor	560R		Various	1206	Chip, thin film	5
R703	Resistor	820R		Various	1206	Chip, thin film	1
RP401, RP402	Resistor array	220R x 8	4816P-1-221LF	Bournes	16 pin SMT		2
RP501	Resistor array	10k x 8	4816P-1-103LF	Bournes	16 pin SMT		1

C304, C305	Capacitor	22pF		Various	1206	Ceramic	2
C606	Capacitor	1nF		Various	1206	Ceramic	1
C605, C610	Capacitor	10nF		Various	1206	Ceramic	2
C101, C102, C103, C104, C105, C106, C107, C201, C202, C203, C204, C205, C206, C211, C213, C301, C302, C303, C401, C402, C403, C404, C501, C502, C503, C601, C602, C603, C607, C702, C703, C704, C705	Capacitor	100nF		Various	1206	Ceramic	33
C108, C208, C209, C210	Capacitor	1uF / 16V		Various	1206	Tantalum	4
C207, C212, C604, C608, C609	Capacitor	10uF / 16V	EEE-1CA100SR	Panasonic	SMT	Electrolytic	5
C611	Capacitor	470uF / 16V	EEE-1CA471UP	Panasonic	SMT	Electrolytic	1
C701	Capacitor	4700uF / 25V		Various	Through hole. Pitch = 7.5mm. Diameter = 16mm.	Electrolytic	1

U104	I.C.		74AC00	Various	SOIC	Quad NAND gate	1
U206, U303	I.C.		74HC00	Various	SOIC	Quad NAND gate	2
U302	I.C.		74HC74	Various	SOIC	Dual flip-flop	1
U301	I.C.		74HC4060	Various	SOIC	14-stage binary counter	1
U205	I.C.		74HCT04	Various	SOIC	Hex inverter	1
U601	I.C.		74HCT08	Various	SOIC	Quad AND gate	1
U102, U103	I.C.		74HCT244	Various	SOIC - WIDE	Octal buffer / driver	2
U501	I.C.		74LS145	Various	SOIC	1-of-10 decoder. OC-outputs	1
U402, U404	I.C.		74LS245	Various	SOIC - WIDE	Octal line driver / receiver	2
U401, U403	I.C.		SN75ALS160	Texas Instruments	SOIC - WIDE	GPIB driver / receiver	2
U201	I.C.		LM555	Various	SOIC	Timer	1
U203	I.C.		AS7C256	Alliance Memory	SOJ	32k x 8 SRAM	1
U202, U204	I.C.		AT27C256	Atmel	DIP	32k x 8 OTP ROM	2
U101	I.C.		W65C02S	WDC	DIP	Microprocessor	1
U105, U107	I.C.		W65C21**N**	WDC	DIP	PIA. DO NOT sub. with W65C21**S**	2
U106	I.C.		W65C22**N**	WDC	DIP	VIA. DO NOT sub. with W65C22**S**	1
U602	I.C.		TL071	Various	SOIC	JFET-input op-amp	1
U603	I.C.		LM386	Texas Instruments	DIP	Audio power amplifier	1
REG701	I.C.		LM317	Various	TO-220	Adjustable positive regulator	1
REG702	I.C.		LM7805	Various	TO-220	+5V fixed regulator	1

B701	Bridge rectifier		W04	Various	TH		1
D201	Diode		LL4148	Various	SOD-80		1
Q501, Q502, Q504, Q505	Transistor		BC850C	Various	SOT-23	NPN	4
Q503, Q506	Transistor		FZT1149A	Diodes Inc.	SOT-223	PNP	2

XTAL301	Crystal	3.93216 MHz		Various	HC-49	12 pF Parallel res.	1
"	Insulator		700-TFL-9001	ECS		Crystal insulator HC-49U/US	1

P201, P301, P601, P602, P603, P701, P702	Connector		0022272041	Molex	TH	KK-254 vertical header, 4-way	7
P502, P503	Connector		0022272061	Molex	TH	KK-254 vertical header, 6-way	2
P401, P501, P504	Connector			Various	TH	26-way IDC boxed header	3
P202	Connector			Various	TH	50-way IDC boxed header	1

HS1, HS2	Heatsink		HSE-B20254-040H	CUI Inc.	TH	25.4x32x20mm w/pin extrusion	2

TO-220 Insulator kit required to isolate REG701 tab from heatsink HS1. REG701 and REG702 mounted with M3 hardware. Sockets recommended for all DIP integrated circuits.

Parts for Video Generator PCB

Designator	Component type	Value	Part #	Manufacturer	Package	Description	Quantity
R3	Resistor	1k		Various	1206	Chip, thin film	1
R1	Resistor	2k2		Various	1206	Chip, thin film	1
R2	Resistor	5k1		Various	1206	Chip, thin film	1
R5, R7, R8, R9, R10, R11, R12	Resistor	10k		Various	1206	Chip, thin film	7
R6	Resistor	68R		Various	1206	Chip, thin film	1
R4	Resistor	220R		Various	1206	Chip, thin film	1
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24	Capacitor	100nF		Various	1206	Ceramic	24
C25, C26, C27, C28	Capacitor	1uF / 16V		Various	1206	Tantalum	4
C29	Capacitor	47uF / 16V	EEE-1CA471UP	Panasonic	SMT	Electrolytic	1
C30	Capacitor	470uF / 16V	EEE-1CA471UP	Panasonic	SMT	Electrolytic	1
U5, U16	I.C.		74HC00	Various	SOIC	Quad NAND gate	2
U6	I.C.		74HC04	Various	SOIC	Hex inverter	1
U4	I.C.		74HC08	Various	SOIC	Quad AND gate	1
U3, U15	I.C.		74HC10	Various	SOIC	Triple 3-input NAND gate	2
U8, U9, U11	I.C.		74HC74	Various	SOIC	Dual flip-flop	3
U2	I.C.		74HC161	Various	SOIC	4-bit binary counter	1
U7, U10	I.C.		74HC4040	Various	SOIC	12-stage binary counter	2
U14	I.C.		74HCT74	Various	SOIC	Dual flip-flop	1
U19, U20, U21	I.C.		74HCT157	Various	SOIC	Multiplexer	3
U12	I.C.		74HCT165	Various	SOIC	Shift register	1
U23, U24	I.C.		74HCT244	Various	SOIC - WIDE	Octal buffer / driver	2
U22	I.C.		AS7C256	Alliance Memory	SOJ	32k x 8 SRAM	1
U13, U17, U18	I.C.		AT27C256	Atmel	DIP	32k x 8 OTP ROM	3
U1	I.C.		MX045-3C-16M0000	CTS Elec. Comp.	DIP	16 MHz oscillator, 14 pin DIP	1
Q1	Transistor		BC860C	Various	SOT-23	PNP	1
P1, P2	Connector		0022272041	Molex	TH	KK-254 vertical header, 4-way	2
P3	Connector			Various	TH	50-way IDC boxed header	1

Parts for Keyboard Interface PCB

Designator	Component type	Value	Part #	Manufacturer	Package	Description	Quantity
R1, R2, R3, R4, R5	Resistor	4k7		Various	1206	Chip, thin film	5
RP1	Resistor array	4k7 x 8	4816P-1-472LF	Bournes	16 pin SMT		1
C2, C3, C4, C5, C6, C7, C8, C9	Capacitor	100nF		Various	1206	Ceramic	8
C1	Capacitor	47uF / 16V	EEE-1CA471UP	Panasonic	SMT	Electrolytic	1
U1, U2	I.C.		PIC16F874A	Microchip	DIP	Microcontroller	2
U3	I.C.		MAX202	Various	SOIC	RS-232 transceiver	1
U4	I.C.		MX045-3C-16M0000	CTS Elec. Comp.	DIP	16 MHz oscillator, 14 pin DIP	1
D1, D2	Diode		BAS85	Various	SOD-80		2
P1	Connector			Various	TH	26-way IDC boxed header	1
P2, P3, P4, P5	Connector		0022272041	Molex	TH	KK-254 vertical header, 4-way	4